GE YAIC Analog I/O Pack

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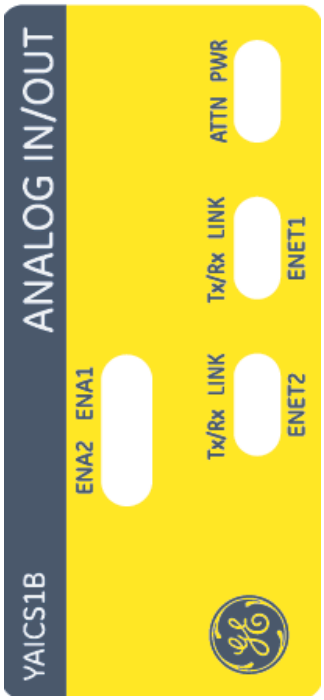
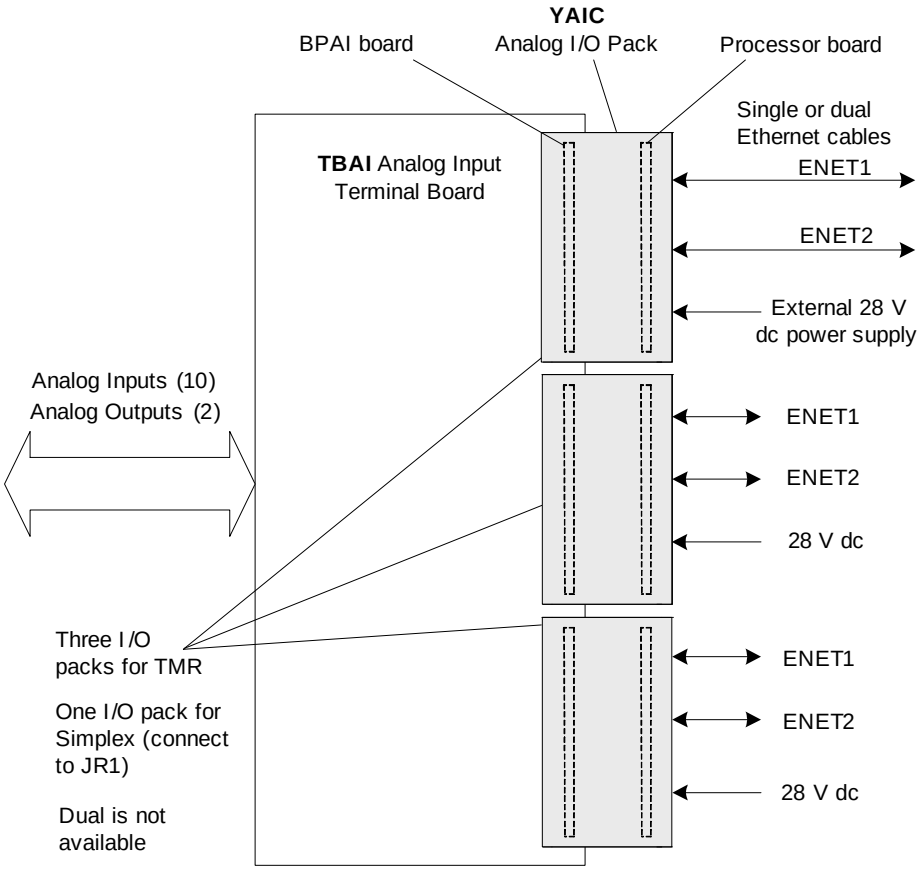
3.2 Mark VIeS YAIC Analog I/O Pack



The Analog I/O pack (IS420YAICS1B) provides the electrical interface between one or two I/O Ethernet networks and an analog I/O terminal board. The YAIC contains a common *processor board* and an acquisition board specific to the analog input function. The I/O pack is capable of handling up to 10 analog inputs, the first eight of which can be configured as ±5 V or ±10 V inputs, or 4-20 mA current loop inputs. The last two inputs can be configured as ±1 mA or 4-20 mA current inputs.

The load terminal resistors for current loop inputs are located on the terminal board and voltage is sensed across these resistors by the YAIC. The I/O pack also includes support for two 0-20 mA current loop outputs. The I/O pack receives or sends data through dual RJ-45 Ethernet connectors to the controller and has a three-pin connector to power it on. Output is through a DC-37 pin connector that connects directly with the associated terminal board connector. Visual diagnostics are provided through indicator LEDs.



3.2.1 YAIC Compatibility

The YAIC I/O pack contains an internal processor board. The following table lists the available versions of the YAIC.

YAIC Version Compatibility

I/O Pack	Processor Board	Compatible (Supported) Firmware	ControlST Software Suite Versions
YAICS1A	BPPB	V04.06	Supported in V04.06 and all later versions
YAICS1B	BPPC	V05.01 and later	Supported in V06.01 and later versions

Attention

YAICS1A and YAICS1B I/O pack versions cannot be mixed on the same T-type terminal board.

All three YAIC I/O packs in a TMR set must be the same hardware form.

To upgrade or replace the YAIC, refer to the following replacement procedures for specific instructions:

- *Replace Mark VIeS Safety I/O Pack with Same Hardware Form*
- *Replace Mark VIeS Safety I/O Pack with Upgraded Hardware Form*

The YAIC I/O pack is compatible with the TBAISIC and STAIS#A terminal boards.

YAIC Terminal Board Compatibility

Terminal Board	Description	I/O Pack Redundancy		
		Simplex	Dual	TMR
TBAIS1C	TMR Analog input/output terminal board	Yes	No	Yes
STAIS#A	Simplex Analog input/output terminal board	Yes	No	No

I/O pack redundancy refers to the number of I/O packs used in a signal path, as follows:

- Simplex uses one I/O pack.
- TMR uses three I/O packs.

3.2.2 YAIC Installation

➢ **To install a new YAIC I/O module into an existing Mark VIeS panel**

1. Securely mount the desired terminal board.
2. Directly plug one YAIC I/O pack for simplex or three YAIC I/O packs for TMR into the terminal board connectors.
3. Mechanically secure the packs using the threaded studs adjacent to the Ethernet ports. The studs slide into a mounting bracket specific to the terminal board type. The bracket location should be adjusted such that there is no right-angle force applied to the DC-37 connector between the pack and the terminal board. The adjustment should only be required once in the life of the product.
4. Plug in one or two Ethernet cables depending on the system configuration. The pack will operate over either port. If dual connections are used, the standard practice is to connect ENET1 to the network associated with the R controller. These choices are also defined in the ToolboxST configuration.
5. Apply power to the pack by plugging in the connector on the side of the pack. It is not necessary to insert this connector with the power removed from the cable as the I/O pack has inherent soft-start capability that controls current inrush on power application.
6. Configure the I/O pack as necessary using the ToolboxST application.

3.2.2.1 Connectors

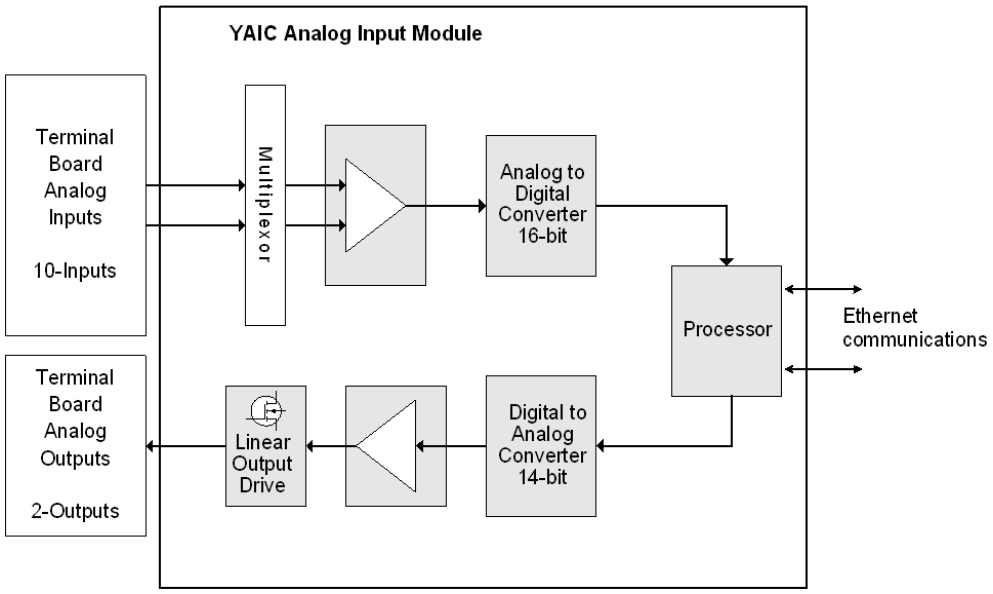
The I/O pack contains the following connectors:

- A DC-37 pin connector on the underside of the YAIC connects directly to the discrete input terminal board. The connector contains the 24 input signals, ID signal, relay coil power, and feedback multiplex command.
- An RJ-45 Ethernet connector named ENET1 on the side of the pack is the primary system interface.
- A second RJ-45 Ethernet connector named ENET2 on the side of the I/O pack is the redundant or secondary system interface.
- A 3-pin power connector on the side of the pack is for 28 V dc power for the pack and terminal board.

3.2.3 YAIC Operation

3.2.3.1 Analog Input Hardware

The YAIC accepts input voltage signals from the terminal board for all 10 input channels. The analog input section consists of an analog multiplexer block, several gain and scaling selections, and a 16-bit analog-to-digital converter (ADC).

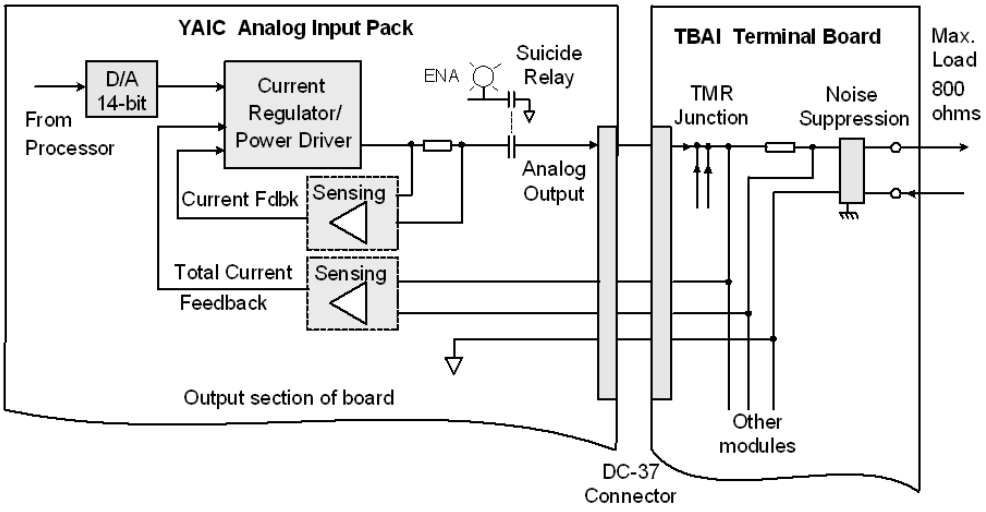


Inputs 1–8 can be individually configured as ±5 V or ±10 V, or 4–20 mA scale signals, depending on the input configuration. Inputs 9–10 can only be configured for ±1 mA or 4-20 mA. The terminal board provides a 250 Ω burden resistor when configured for current inputs yielding a 5 V signal at 20 mA. These analog input signals are first passed through a passive, low pass filter network with a pole at 75.15 Hz. Voltage signal feedbacks from the analog output circuits and calibration voltages are also sensed by the YAIC analog input section.

3.2.3.2 Analog Output Hardware

The YAIC includes two 0-20 mA analog outputs capable of 18 V compliance running simplex or TMR. A 14-bit digital-to-analog converter (DAC) commands a current reference to the current regulator loop in the YAIC that senses current both in the YAIC pack and on the terminal board. In TMR mode, the three current regulators in each YAIC share the commanded current loads among themselves. Analog output status feedbacks for each output include:

- Current reference voltage
- Individual current (output current sourced from within the YAIC)
- Total current (as sensed from the terminal board, summed current in TMR mode)



Each analog output circuit also includes a normally open mechanical relay to enable or disable operation of the output. The relay is used to remove a failed output from a TMR system allowing the remaining two YAICs to create the correct output without interference from the failed circuit. When the suicide relay is de-activated, the output opens through the relay, open-circuiting the analog output from the customer load that is connected to the terminal board. The mechanical relay has a second normally open contact that is used as a status to indicate position of the relay to the control and includes visual indication with an LED.

3.2.4 Specifications

Item	YAIC Specification
Number of Cchannels	12 channels per terminal board (10 AI, 2 AO)
AI Types Supported	Inputs 1 to 8: ±5 V dc, ±10 V dc, or 4–20 mA Inputs 9 to 10: 4–20 mA or ±1 mA
Input Converter Resolution	16-bit ADC
Scan Time	Normal scan 5 ms (200 Hz) *The update rate in the controller is based on the frame rate.*
Input Accuracy	0.1% of full scale over the full operating temperature range.
Noise Suppression on Inputs	The 10 circuits have hardware filter with single pole down break at 500 rad/s. A software filter, using a two pole low pass filter, is configurable for: 0.75 Hz, 1.5 Hz, 3 Hz, 6 Hz, 12 Hz
Common Mode Rejection	AC CMR 60 dB at 60 Hz, with up to ±5 V common mode voltage. DC CMR 80 dB with -5 to +7 peak V common mode voltage
Common Mode Voltage Range	±5 V (±2 V CMR for the ±10 V inputs)
Output Converter	14-bit D/A converter with 0.5% accuracy
Output Load	800 Ω max for 4-20 mA output
Output Accuracy	±0.5% of full measurement range
Power Consumption	5.3 watts typical, 6.2 watts worst case
Compressor Stall Detection	Not supported
Size	8.26 cm high x 4.19 cm wide x 12.1 cm deep (3.25 in x 1.65 in x 4.78 in)
Ambient Rating for Enclosure Design†	-30 to 65 ºC (-22 to 149 ºF)
Technology	Surface mount

Note † For further details, refer to the *Mark VIe and Mark VIeS Control Systems Volume I: System Guide* (GEH-6721_Vol_I), the chapter *Technical Regulations, Standards, and Environments*.

3.2.5 YAIC Diagnostics

The PAIC or YAIC performs the following self-diagnostic tests:

- A power-up self-test that includes checks of RAM, flash memory, Ethernet ports, and most of the processor board hardware
- Continuous monitoring of the internal power supplies for correct operation
- A check of the electronic ID information from the terminal board, acquisition board, and processor board to confirm that the hardware set matches, followed by a check that the application code loaded from flash memory is correct for the hardware set
- Each analog input has hardware limit checking based on configurable high and low levels for 4-20 mA inputs and preset (non-configurable) levels for ± 5 V, ± 10 V, and ± 1 mA inputs. If the limit is exceeded, then the I/O pack raises an alarm and marks the input as unhealthy. A logic signal (L3DIAG_pack) is set, which refers to the entire board.
- Each input has configurable system limit checking with high and low levels, latching, and non-latching selection options. These limits can be used in the programming of the controller to generate process alarms. This controller logic requires using a RSTSYS pin on a SYS_OUTPUTS block to reset the out of limits status when the latch is enabled. System limit checking can be configured as Enable/Disable at point level, and are only functional only when system limits are enabled at module level (Parameters tab).
- The analog input hardware includes precision reference voltages in each scan. Measured values are compared against expected values and are used to confirm health of the analog to digital converter circuits.
- Analog output current is sensed on the terminal board using a small burden resistor. The I/O pack conditions this signal and compares it to the commanded current to confirm health of the digital to analog converter circuits.
- The analog output suicide relay is continuously monitored for agreement between commanded state and feedback indication.

Details of the individual diagnostics are available from the ToolboxST application. The diagnostic signals can be individually latched and then reset with the RSTDIAG signal if they go healthy.

The application status diagnostic LEDs are provided in the following table.

Relay Application Status LEDs

LED	Label	Description
Yellow	ENA1	Closure of the relay controlling output 1
Yellow	ENA2	Closure of the relay controlling output 2

3.2.6 YAICS1B Configuration

3.2.6.1 Parameters

Parameter	Description	Choices
SystemLimits	Enable or *temporarily* disable all system limit checks. Setting this parameter to Disable will cause a diagnostic alarm to occur.	Enable, Disable
Min_ MA_Input	Select minimum current for healthy 4-20 mA input	0 to 22.5 mA
Max_ MA_Input	Select maximum current for healthy 4-20 mA input	0 to 22.5 mA

3.2.6.2 Inputs

Input	Description	Choices
AnalogInput01 through AnalogInput10	First of 10 Analog Inputs – board point. Point edit	(Input REAL)
InputType	Current or voltage input type	Unused or 4-20 mA (for all Analog Inputs) ±5 V or ±10 V (for AnalogInput01 to 08 only) ±1 mA (for AnalogInput09 and 10 only)
Low_Input	Value of input current (mA) or voltage (V) at low end of input scale	-10 to 20
Low_Value	Value of input in engineering units at Low_Input	-3.4082 e + 038 to 3.4028 e + 038
High_Input	Value of input current (mA) or voltage (V) at high end of input scale	-10 to 20
High_Value	Value of input in engineering units at High_Input	-3.4082 e + 038 to 3.4028 e + 038
InputFilter	Bandwidth of input signal filter	Unused, 0.75hz, 1.5hz, 3hz, 6hz, 12hz
TMR_DiffLimit	Difference limit for voted inputs in % of High_Value - Low_Value	0 to 200
SysLim1Enabl	Enable System Limit 1 fault check	Enable, Disable
SysLim1Latch	System Limit 1 fault latch - if set, requires a Reset System Limits (RSTSYS) on SYS_OUTPUTS block to clear	Latch, NotLatch
SysLim1Type	System Limit 1 Check Type	>= or <=
SysLim1	System Limit 1 in engineering units	-3.4082 e + 038 to 3.4028 e + 038
SysLim2Enabl	Enable System Limit 1 fault check	Enable, Disable
SysLim2Latch	System Limit 2 fault latch - if set, requires a Reset System Limits (RSTSYS) on SYS_OUTPUTS block to clear	Latch, NotLatch
SysLim2Type	System Limit 2 Check Type	>= or <=
SysLimit2	System Limit 2 in Engineering Units	-3.4082 e + 038 to 3.4028 e + 038
DiagHighEnab	Enables the generation of a high limit diagnostic alarm when the value of the 4-20 mA input is greater than the value of parameter *Max_MA_Input*	Enable, Disable
DiagLowEnab	Enables the generation of a low limit diagnostic alarm when the value of the 4-20 mA input is less than the value of parameter *Min_ MA_Input*	Enable, Disable
TMR_DiffLimt	Diag limit, TMR input vote difference, in percent of (High_Value - Low_Value)	0 to 200 %

3.2.6.3 Outputs

Output Name	Output Description	Choices
AnalogOutput01 - AnalogOutput02	First of two analog outputs - board point, Point edit	Output REAL
Output_MA	Output current, mA selection.	Unused, 0-20 mA
OutputState	State of the outputs when offline. When the PAIC loses communication with the controller, this parameter determines how it drives the outputs: PwrDownMode - Open the output relay and drive outputs to zero current HoldLastVal - Hold the last value received from the controller Output_Value - Go to the configured output value set by the parameter Output_Value	PwrDownMode HoldLastVal Output_Value
Output_Value	Pre-determined value for the outputs	-3.4082 e + 038 to 3.4028 e + 038
Low_MA	Output mA at low value	0 to 200 mA
Low_Value	Output in Engineering Units at Low_MA	-3.4082 e + 038 to 3.4028 e + 038
High_MA	Output mA at high value	0 to 200 mA
High_Value	Output value in Engineering Units at High_MA	-3.4082 e + 038 to 3.4028 e + 038
TMR_Suicide	Enables suicide for faulty output current, TMR only	Enable, Disable
TMR_SuicLimit	Suicide threshold (Load sharing margin) for TMR operation, in mA	0 to 200 mA
D/A_ErrLimit	Difference between D/A reference and feedback, in % for suicide, TMR only	0 to 200 %
Dither_Ampl	Dither % current of Scaled Output mA	0 to 10
Dither_Freq	Dither rate in Hertz	Unused, 12.5hz, 25hz, 33.33hz, 50hz, 100hz

3.2.6.4 Variables

Variable Name	Description	Direction	Type
L3DIAG_YAIC	Board diagnostic	Input	BOOL
LINK_OK_YAIC	I/O Link OK indication	Input	BOOL
ATTN_YAIC	Module Diagnostic	Input	BOOL
IOPackTmpr	I/O Pack Temperature (deg F)	Input	REAL
PS18V_YAIC	I/O 18V Power Supply Indication	Input	BOOL
PS28V_YAIC	I/O 28V Power Supply Indication	Input	BOOL
SysLimit1_1	System Limit 1	Input	BOOL
↓	↓	Input	BOOL
SysLimit1_10	System Limit 1	Input	BOOL
SysLimit2_1	System Limit 2	Input	BOOL
↓	↓	Input	BOOL
SysLimit2_10	System Limit 2	Input	BOOL
OutSuicide1	Status of Suicide Relay for Output 1	Input	BOOL
OutSuicide2	Status of Suicide Relay for Output 2	Input	BOOL
Out1MA	Feedback, Total Output Current, mA	Input	REAL
Out2MA	Feedback, Total Output Current, mA	Input	REAL