GE PPRO, YPRO Backup Turbine Protection

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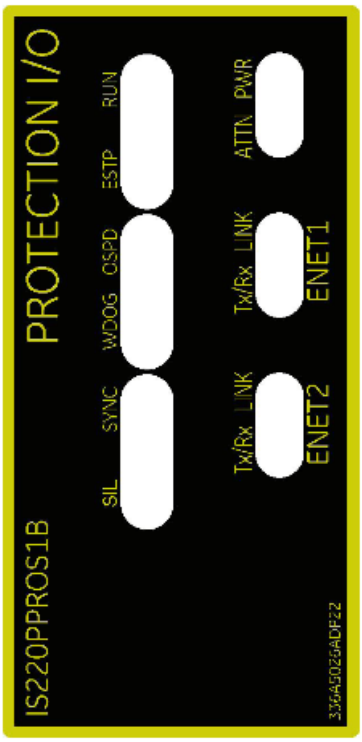
7 PPRO, YPRO Backup Turbine Protection

7.1 Mark VIe PPRO Backup Turbine Protection I/O Pack



The Backup Turbine Protection (PPRO) I/O pack and associated terminal boards provide an independent backup overspeed protection system with a backup check for generator synchronization to a utility bus. They also provide an independent watchdog function for the primary control. A typical protection system consists of three triple modular redundant (TMR) PPRO I/O packs mounted to a separate simplex protection (SPRO) terminal board or three PPROs mounted on a TMR TPROH#C terminal board. A cable, with DC-37 pin connectors on each end, connects each SPRO or TPROH#C to the designated emergency trip board:

- TREG: Gas Turbine Emergency Trip Terminal Board
- TREL: Large Steam Turbine Emergency Trip Terminal Board
- TRES: Small/Medium Steam Turbine Emergency Trip Terminal Board

An alternate arrangement puts three PPRO I/O packs directly on TREA for a single-board TMR protection system. The PPRO has an Ethernet connection for IONet communications with the control modules.

The Mark* VIe control is designed with a primary and backup trip system that interacts at the trip terminal board level. Primary protection is provided with the Turbine Primary I/O pack (PTUR) operating a primary trip board (TRPG, TRPL, TRPS, TRPA). Backup protection is provided with the PPRO I/O pack operating a backup trip board (TREG, TREL, TRES, TREA).

The PPRO accepts three speed signals for overspeed protection functions, including basic overspeed, acceleration, deceleration, and a hardware implemented overspeed. The I/O pack monitors the operation of the primary control and can monitor the primary speed as a sign of normal operation. The PPRO monitors the status and operation of the selected trip board through a comprehensive set of feedback signals. If a problem is detected, the PPRO activates the backup trip relays on the trip board and activates a trip on the primary control. The I/O pack is fully independent of and unaffected by the primary control operation.

A maximum of three trip solenoids can be connected between the primary and emergency trip terminal boards. Connecting a solenoid between the boards isolates the power on both sides of the solenoid as well as visibility of solenoid voltage as a system feedback. The primary/emergency trip boards TRPG/TREG, TRPL/TREL, and TRPS/TRES are designed to operate as a pair and use cabling between the boards for system connections. The TRPA and TREA are designed with no pairing required and can be used independently of each other. When TRPA and TREA are paired, they function the same as other board pairs.

7.1.1 Compatibility

The PPRO I/O pack includes one of the following compatible BPPx processor boards:

- The PPROH1A contains a BPPB processor board.
- The PPROS1B contains a functionally compatible BPPC processor board that is supported in the ControlST* software suite V04.07 and later.

The PPROS1B is an IEC 61508 certified version for use in IEC 61511 certified safety loops. The safety-certified I/O pack, trip board, and terminal board combinations are as follows:

- PPROS1B, TPROS#C, TREGS1B, 125 V dc
- PPROS1B, TPROS#C, TREGS2B, 24 V dc
- PPROS1B, TPROS#C, TREGS3B, 125 V dc, TMR, special 28 V power JX1
- PPROS1B, TPROS#C, TREGS4B, 125 V dc , TMR, special 28 V Power JY1
- PPROS1B, TPROS#C, TREGS4B, 125 V dc , TMR, special 28 V Power JZ1

Note Refer to the *Mark VIe Control PPROS1B and PPRAS1x Functional Safety Instruction Guide* (GEI-100709).

The PPRO I/O pack mounts directly to the SPRO, TPROS#C, TPROH#C, or TREA. When mounted on the SPRO or TPRO, it is cable-compatible to the TREG, TREL, or TRES trip board.

Trip Board Compatibility

Board[1]	TMR	Simplex	Output Contacts, 125 V dc	Output Contacts, 24 V dc	E-Stop	Input Contacts, 125 V dc	Input Contacts, 24 V dc	Economy Resistor
TREG_1B	Yes	No	Yes	Yes	Yes	Yes	No	Yes
TREG_2B	Yes	No	Yes	Yes	Yes	No	Yes	Yes
TREG_3B[2]	Yes	No	Yes	Yes	Yes	Yes	No	Yes
TREG_4B[2]	Yes	No	Yes	Yes	Yes	Yes	No	Yes
TREG_5B[2]	Yes	No	Yes	Yes	Yes	Yes	No	Yes
TRELH1A	Yes	No	Yes	Yes	No	Yes	No	No
TRELH2A	Yes	No	Yes	Yes	No	No	Yes	No
TRESH1A	Yes	Yes	Yes	Yes	No	Yes	No	No
TRESH2A	Yes	Yes	Yes	Yes	No	No	Yes	No
TREAH1A	Yes	No	No	Yes	Yes	No	No	No
TREAH2A	Yes	No	Yes	No	Yes	No	No	No
TREAH3A[3]	Yes	No	No	Yes	Yes	No	No	No
TREAH4A[3]	Yes	No	Yes	No	Yes	No	No	No
TREAS1A[3]	Yes	No	Yes	No	Yes	No	No	No
TREAS2A[3]	Yes	No	Yes	No	Yes	No	No	No
TREAS3A[3]	Yes	No	Yes	No	Yes	No	No	No
TREAS4A[3]	Yes	No	Yes	No	Yes	No	No	No

[1] Underscore (_) indicates the TREG board version may be H or S.

[2] The TREG_3A, 4A, and 5A versions are the same as the 1A except that power is provided by JX1, JY1, or JZ1.

[3] TREA_#A and _#A are the same as _1A and _2A only Euro versions.

7.1.1.1 Simplex Main Control

Simplex backup protection is supported by the Mark VIe control trip board TRES. One PPRO network port resides on the controller IONet.

TMR backup protection is supported by all Mark VIe control backup trip boards, TREG, TREL, TREA, and TRES. In this configuration, each I/O pack is connected to a separate (R,S,T) controller network.

7.1.1.2 Dual Main Control

Simplex backup protection is supported by the Mark VIe control trip board TRES. When used in this configuration, the first network connection is to the R controller. The second network connection is to the S controller. The PPRO is then responsible for monitoring the operation of both controllers. The PPRO supports two options: the pack trips if either controller malfunctions or if both controllers malfunction.

TMR backup protection is supported by all Mark VIe control backup trip boards, TREG, TREL, TREA, and TRES. This configuration uses the dual controller TMR output standard network connection. The first PPRO has one network port connected to the R controller network. The second I/O pack has one network port connected to the S controller network. The third pack has one network port connected to the R controller network and one network port connected to the S controller network. The third PPRO monitors the operation of both controllers. The I/O pack activates a trips if either controller malfunctions or both controllers malfunction.

7.1.1.3 Triple Main Control

TMR backup protection is supported when operating with a TMR main control (two out of three running). All Mark VIe control backup trip boards (TREG, TREL, TREA, and TRES) support this configuration. The normal network configuration connects the first PPRO I/O pack to the R network, the second PPRO to the S network, and the third PPRO to the T network.

PPRO TMR applications do not support dual network connections for all three PPROs. In a redundant system there is no additional system reliability gained by adding network connections to the first two PPROs with dual controllers or any of the three PPROs with TMR controllers. The additional connections simply reduce mean time between failures (MTBF) without increasing mean time between forced outages (MTBFO).

Note Simplex backup protection is not supported. One PPRO cannot monitor the health of all three main controls and trip on loss of a single main control. Therefore, one of the fundamental protection features cannot be met with a single I/O pack.

7.1.2 Installation

The PPRO I/O pack mounts directly to the SPRO, TPROS#C, TPROH#C, or TREA. When mounted on the SPRO or TPROH#C, cables with DC-37 pin connectors on both ends are required between the SPRO or TPROH#C and the selected trip terminal board.

➢ **To install the PPRO I/O pack**

1. Securely mount the SPRO, TPROH#C, or TREA terminal board. Mount the selected trip terminal board if SPRO or TPRO is used.
2. Connect the cable with DC-37 pin connectors on each end between the SPRO or TPRO and the selected trip terminal board (if TREA is not used).
3. Directly plug one PPRO into each SPRO, or three PPROs into the TREA or TPRO.
4. Slide the threaded posts on PPRO, located on each side of the Ethernet ports, into the slots on the terminal board mounting bracket. Adjust the bracket location so the DC-62 pin connector on PPRO and the terminal board fit together securely. Tighten the mounting bracket. The adjustment should only be required once in the service life of the product. Securely tighten the nuts on the threaded posts locking PPRO in place.
5. Plug in one or two Ethernet cables depending on the system configuration. The PPRO module is not sensitive to Ethernet connections and selects the proper operation over either port.
6. Apply power to the module by plugging in the power connector on the side of the module. The I/O module has inherent soft-start capability that controls current levels upon application.
7. Use the ToolboxST* application to configure the module as necessary. For more information, refer to *GEH-6700, ToolboxST User Guide for Mark VIe Control.*

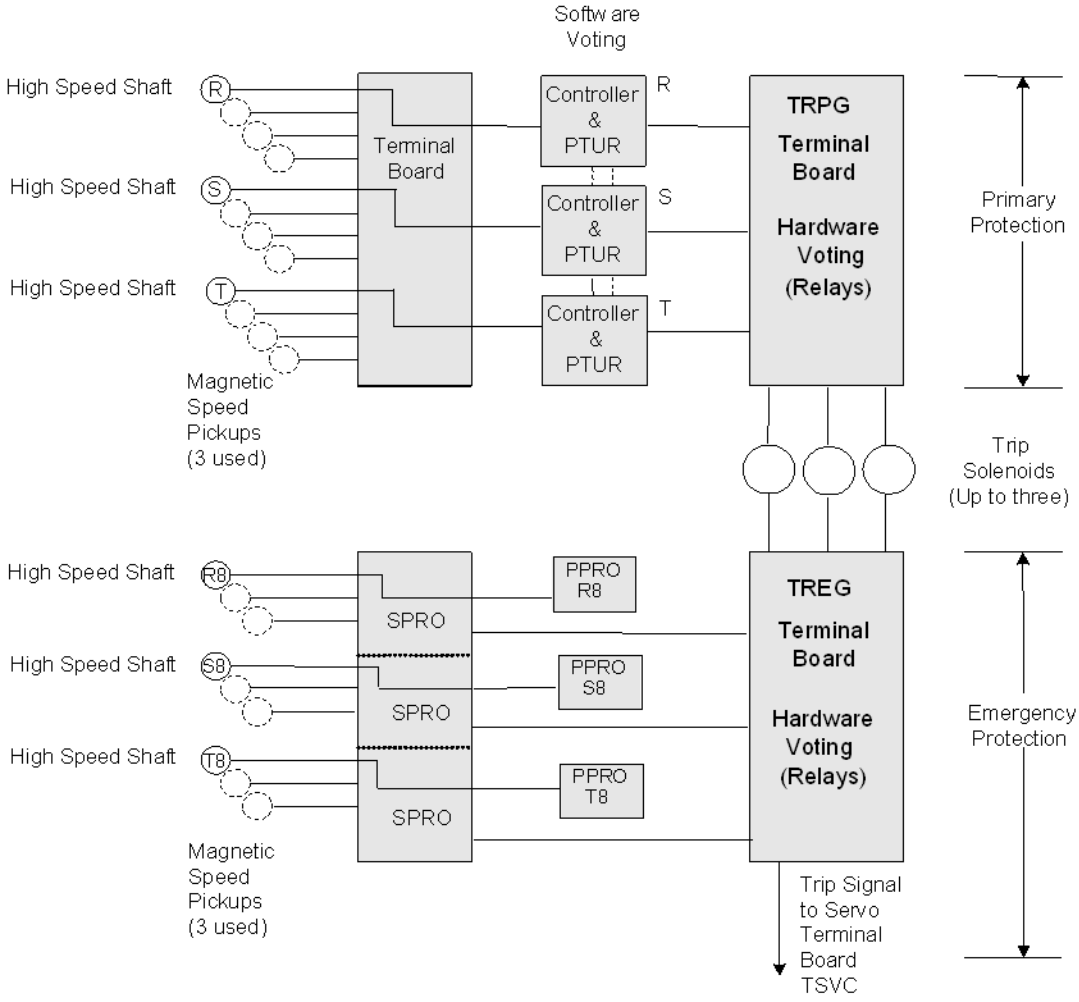
7.1.3 Operation

Refer to the following sections in the *GEH-6721_Vol_II*, the chapter, *Common Module Content*:

- *Auto-reconfiguration*
- *BPPx Processor*
- *Processor LEDs*
- *Power Management*
- *ID Line*
- *Common Module Alarms*

7.1.3.1 Overspeed Protection

Turbine overspeed protection is available in three levels; control, primary, and emergency. Control protection comes through closed loop speed control using the fuel/steam valves. Primary overspeed protection is provided by the controller. The TTUR terminal board and PTUR I/O pack bring in a shaft speed signal to each controller where the median signal is selected. If the controller determines a trip condition, it sends the trip signal to the TRPG terminal board through the PTUR I/O board. The three PTUR outputs are 2/3 voted in three relay voting circuits (one for each trip solenoid) and power is removed from the solenoids. The following figure displays the primary and emergency levels of protection.



Primary and Emergency Overspeed Protection

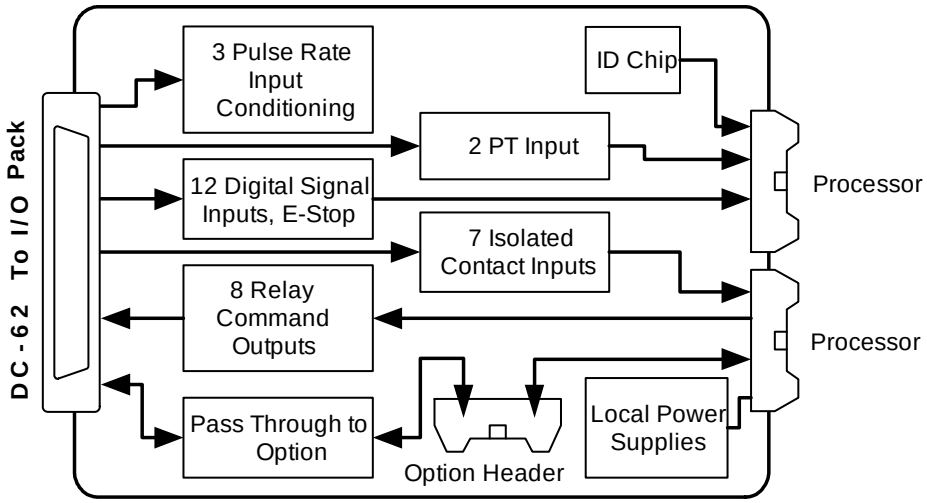
Emergency overspeed protection is provided by the independent triple redundant PPRO protection system displayed in the preceding figure. This uses three shaft speed signals from magnetic pickups (MPU), one for each protection module. These are brought into SPRO, a terminal board dedicated to the protection system.

Each PPRO independently determines when to trip, and the signals are passed to the TREG terminal board. TREG operates in a similar way to TRPG, voting the three trip signals in relay circuits and removing power from the trip solenoids. This system contains no software voting, making the three PPRO modules completely independent. The only link between PPRO and the other parts of the control system is the IONet cable, which transmits status information.

Additional protection for simplex systems is provided by the protection module through the Servo Terminal Board, TSVC. Plug J1 on TREG is wired to plug JD1 on TSVC, and if this is energized, relay K1 disconnects the servo output current and applies a bias to force the control valve closed.

7.1.3.2 Application-specific Hardware

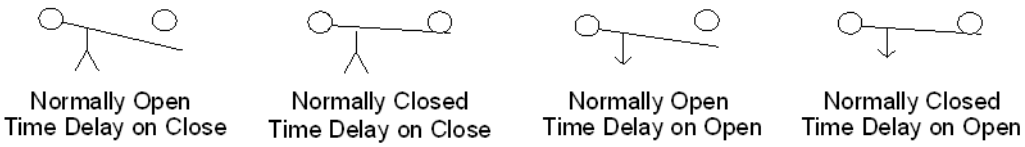
The I/O pack has an internal, application-specific circuit board (BPRO) that contains the hardware needed for the turbine backup trip function. The application board connects between the processor and either the SPRO, TPRO, or TREA terminal board. The application board has provisions for additional hardware expansion options that can be added through a dedicated header.



BPRO Application Board

7.1.3.3 Protective Functions

The I/O pack performs the following protective functions in a mix of hardware, programmable logic, and firmware. In the following diagram, standard symbols for time delay contacts have been used:



In the following diagrams, a standard has been used to indicate signal origin and flow.

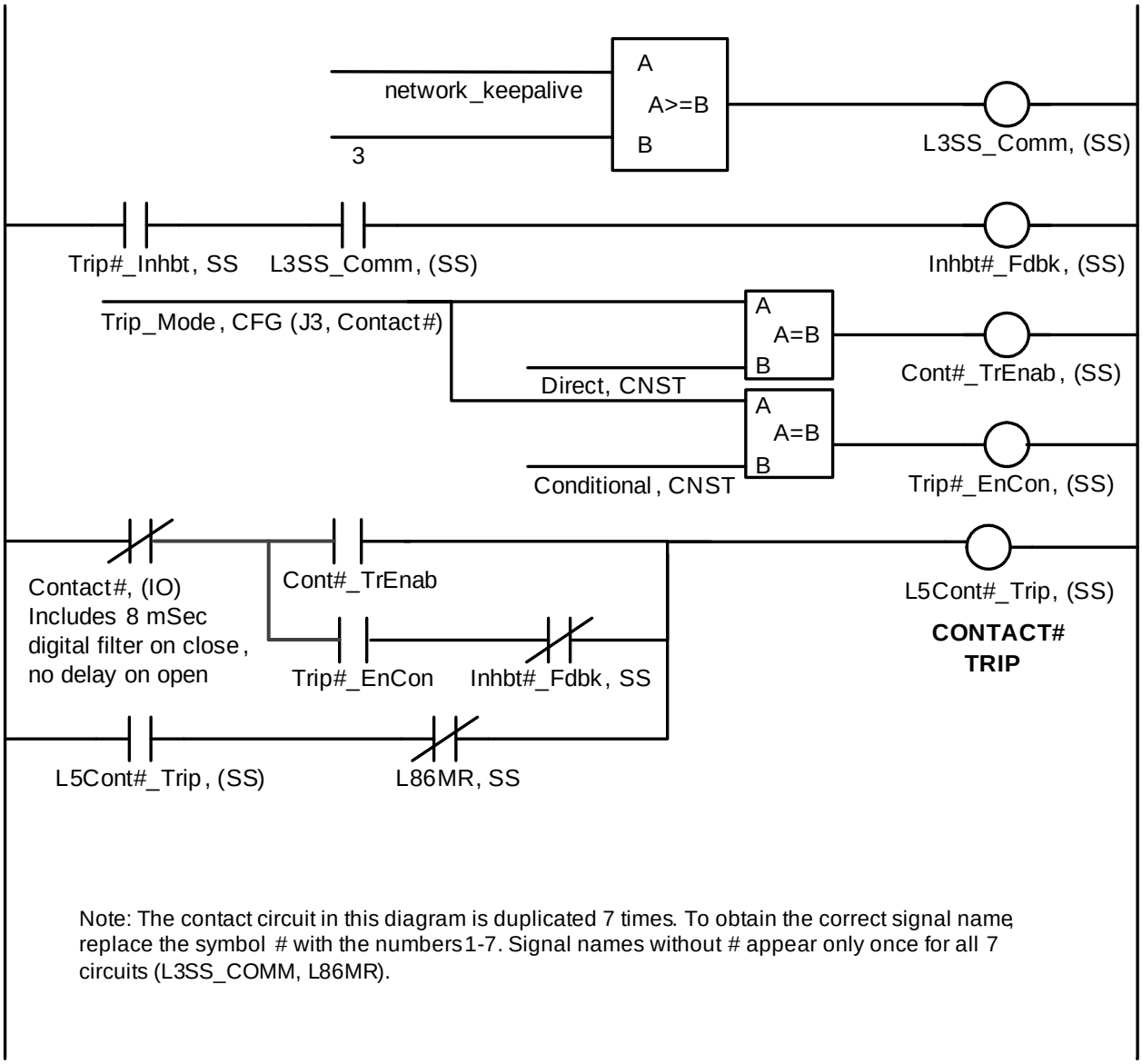
- Signal names that end with (SS) are created within the I/O pack and the data flow is out to the controller through signal space.
- Signal names that end with SS are created in the controller and the data flow is into the I/O pack through signal space.
- Signal names that end with (IO) are created within the I/O pack and the data flow is out to the hardware.
- Signal names that end with IO indicate the signal is a hardware input into the I/O pack.
- Signal names that end with anything containing CFG are part of the I/O pack configuration. In this case an attempt has been made to indicate what area of the I/O pack configuration contains the variable.
- When J3 is referenced in a CFG, it refers to the connection point for the turbine backup trip relay board, and the corresponding configuration values.
- The combination IO (SS) indicates a signal that comes from the hardware inputs to the I/O pack, and is then sent out to the controller as part of signal space.

If there is no special ending on a signal name, then the signal is used internal to the I/O pack and is not part of the hardware or signal-space data movement. This signal is not available or visible to applications, but it is needed to adequately describe the I/O pack's operation.

7.1.3.4 Direct/Conditional Discrete Input Trip

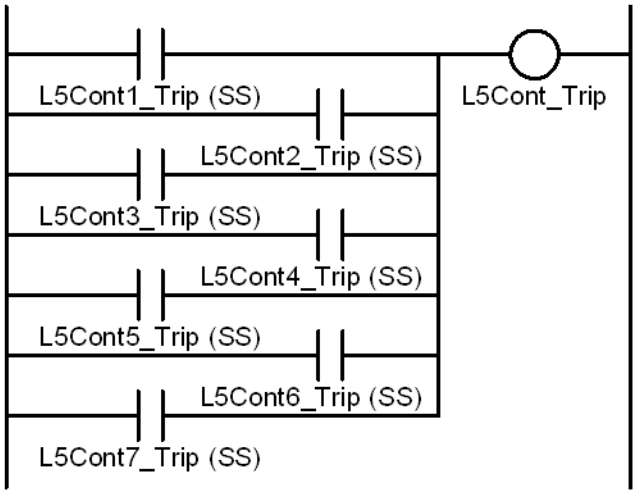
The I/O pack supports the seven isolated discrete contact input trip signals provided on the backup turbine trip board. In the following figure, the direct / conditional determination is implemented in firmware while Contact#, and L5Cont#_Trip are in hardware logic. When configured for direct trip, the firmware is not in the trip path. When configured for conditional trip, the firmware determines the communication health (displayed as network_keepalive) and populates the programmable logic with the conditional signal from signal space. If the controller communication is lost, the default will permit any conditional trip.

Note The contact inputs include an 8 ms contact de-bounce filter to protect against false trips.



Contact Input Trips

The resulting contact trip signals are combined into a single contact trip summary, L5Cont_Trip.

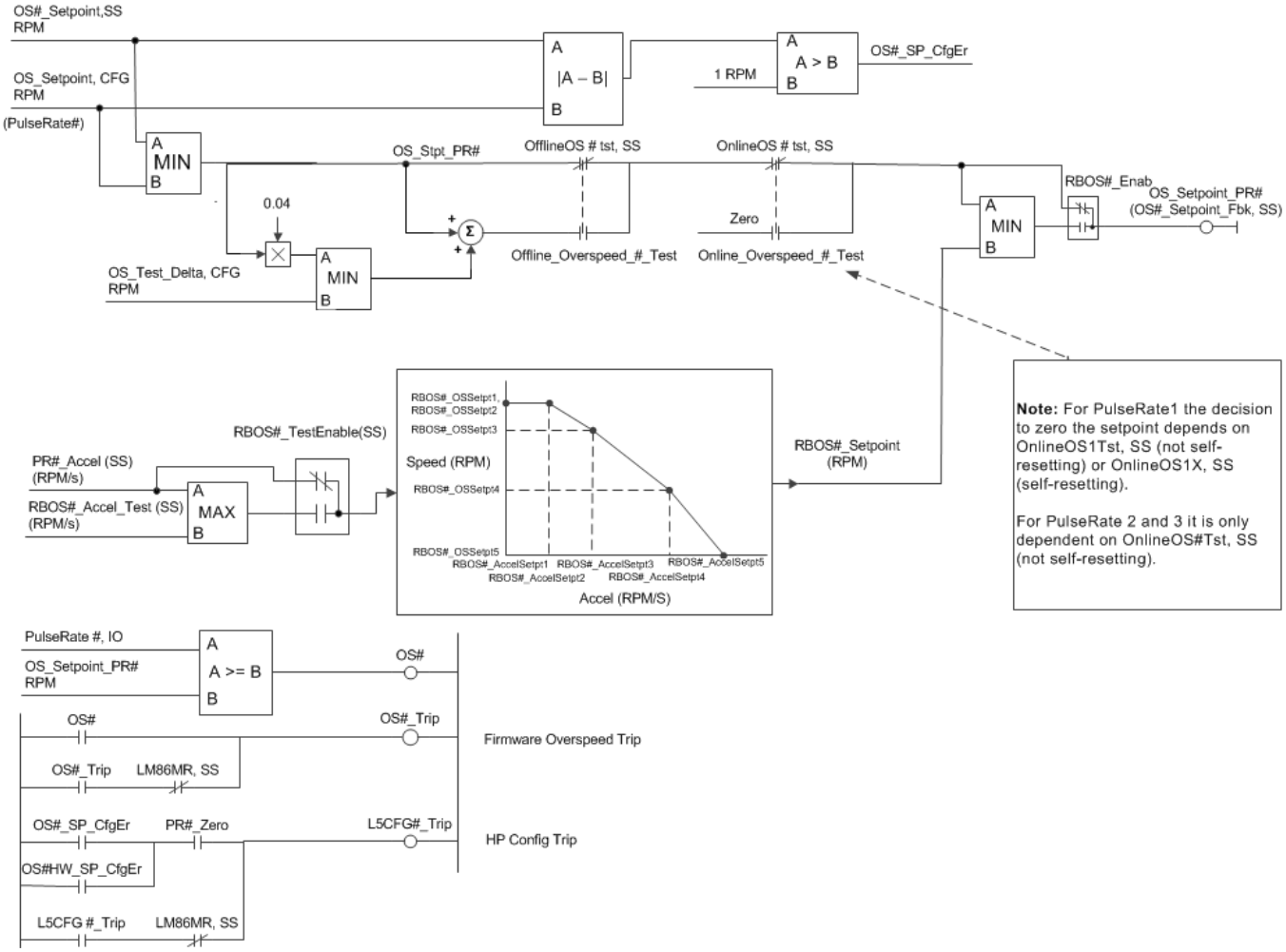


Contact Input Trip Signal Concentration

7.1.3.5 Firmware Overspeed Trip

Firmware overspeed protection is performed on the three values that come out of the high speed select. Although the established standard for naming these three inputs is HP, IP, and LP, the three inputs are free to be applied as needed in a system design.

Note The following pulse rate variables are displayed using a # symbol. Replace the # with 1 for HP, 2 for LP, or 3 for IP.



Firmware Overspeed

Firmware Overspeed Trip functions include:

- Fault on overspeed threshold match failure between config and signal space values when speed is zero
- Pick the lower threshold from config or signal space
- Provide a mechanism to zero the threshold for online overspeed test
- Provide a mechanism to modify the threshold for offline overspeed test, bounded to limit increases to the threshold to 104%
- Provide a mechanism to modify the threshold based upon current computed acceleration (Rate-based Overspeed feature). Refer to the section *Rate-Based Overspeed Trip (RBOS)*.

Note Use a negative OS_Tst_Delta value to reduce the threshold during testing.

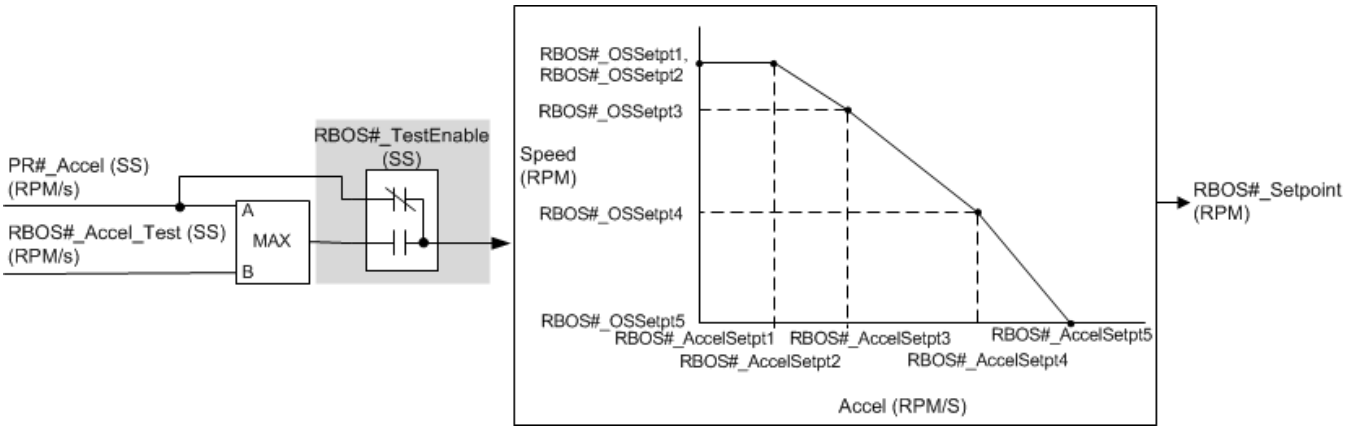
- Compare the threshold to the calculated speed and latch overspeed
- Active firmware overspeed setpoint (OS_Setpoint_PR#) is available as an input signal

Rate-based Overspeed Trip (RBOS)

Note Rate-based Overspeed is only supported on PPROS1B. RBOS cannot be enabled if a PPROH1A I/O pack is configured.

The Rate-based Overspeed (RBOS) function is an optional feature that is implemented for each shaft independently. It enables the PPRO to modify the firmware overspeed threshold trip setpoint in real-time based upon the current acceleration of the shaft. The purpose of the RBOS feature is to specify an overspeed setpoint profile that lowers the firmware overspeed setpoint dynamically as the shaft acceleration increases. The user has the ability to enable or disable the RBOS feature on a per-shaft basis, and can specify the response curve per shaft. There is also a Test mode that allows the user to insert a test acceleration input to the function.

The core of the RBOS feature is a user-specified overspeed setpoint profile composed of five acceleration and overspeed setpoint breakpoints. These breakpoints define a response curve, with the X-axis as acceleration in RPM/s, and the Y-axis as Overspeed setpoint in RPM. The RBOS feature interpolates between these breakpoints to provide an RBOS-driven overspeed setpoint given an input acceleration. The following diagram illustrates this overspeed setpoint profile.



RBOS Overspeed Setpoint Profile

As shown in the *Firmware Overspeed* diagram, some simple logic chooses which acceleration to use in the RBOS feature. If the RBOS#_TestEnable is *True*, then the RBOS#_Accel_Test is used as Accel input for RBOS, unless the actual acceleration (PR#_Accel) is greater.

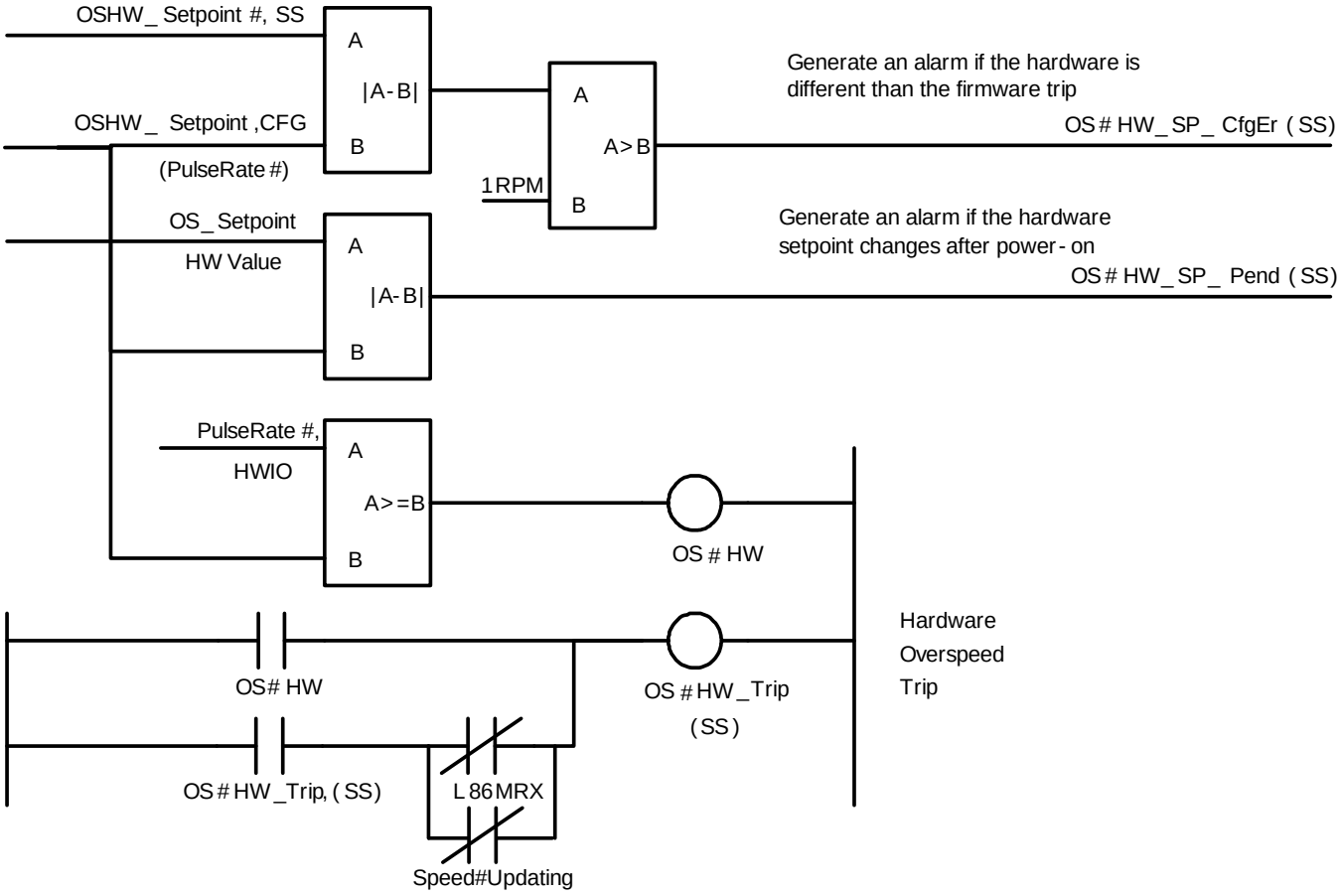
The chosen acceleration is fed into the overspeed setpoint profile and a calculated RBOS#_Setpoint is provided. If the acceleration is less than RBOS#_AccelSetpt1 or greater than RBOS#_AccelSetpt5, the RBOS#_Setpoint is clamped to be equal to RBOS#_OSSetpt1 or RBOS#_OSSetpt5 respectively. Thus, the overspeed setpoint profile does not extrapolate past the setpoint range, but instead clamps the output.

Once the RBOS overspeed setpoint profile has calculated a RBOS#_Setpoint, the result is minimum-selected against the firmware overspeed output from the rest of the firmware overspeed logic if the RBOS feature is enabled (RBOS#_Enab). This final selected overspeed setpoint (OS_Setpoint_PR#) is compared against the PulseRate# shaft speed to drive an overspeed trip. It is also available to the user in signal space as OS#_Setpoint_Fbk.

Note Refer to the section *Parameters* for details on configuration parameters for the RBOS feature, and the section *Variables Vars-Speed* for details on RBOS I/O signals.

7.1.3.6 Hardware Overspeed Trip

The following pulse rate variables are displayed using a # symbol. Replace the # with 1 for HP, 2 for LP, or 3 for IP. OSHW_ Setpoint only goes into the hardware at I/O pack startup.



Hardware Overspeed Trip, HP Shaft

Note Refer to the section *Shaft Speed Accel, Decel, and Zero* for the definition of Speed#Updating.

Hardware Overspeed Trip functions include:

- Load the independent hardware overspeed set point only when the I/O pack restarts or is power cycled
- Generate an alarm when the hardware configuration set point is >1 Hz different from the value passed through signal space from the application configuration

Note Hardware overspeed detection involves two rotations of the shaft to determine an overspeed condition.

- Generate an alarm and signal space Boolean when the set point in configuration fails to match the value stored in the hardware
- Implement speed calculation and the trip logic entirely inside programmable logic
- Overspeed trip response typically less than 60 ms at normal operating speeds

Note There is no separate enable or disable signal for this overspeed protection. The disable signal is created by setting a high overspeed point value. The calculated speed will never reach the value needed to trigger OS1HW.

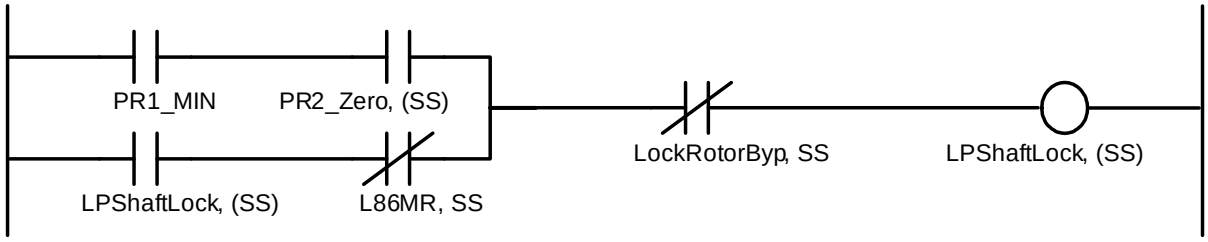
The actual hardware implementation depends on two configuration items:

- **OSHW_Setpoint** specifies the overspeed trip level in RPM.
- **PRScale** determines the number of speed sensor pulses per revolution used to convert pulse rate into RPM for both hardware and firmware overspeed value.

The hardware implementation requires two adjacent revolutions exceeding the OSHW_Setpoint to trip the system. When a trip is present, the setting of OSHW_Setpoint is reduced by a small amount in the hardware to provide a clean trip signal. Due to this reduction, speed must be reduced well below the overspeed threshold before a reset may take place. Because there are set limits to the time integration used in the hardware detector, the minimum RPM setting for the OSHW_Setpoint is approximately four RPM.

7.1.3.7 LP Shaft Locked Detection

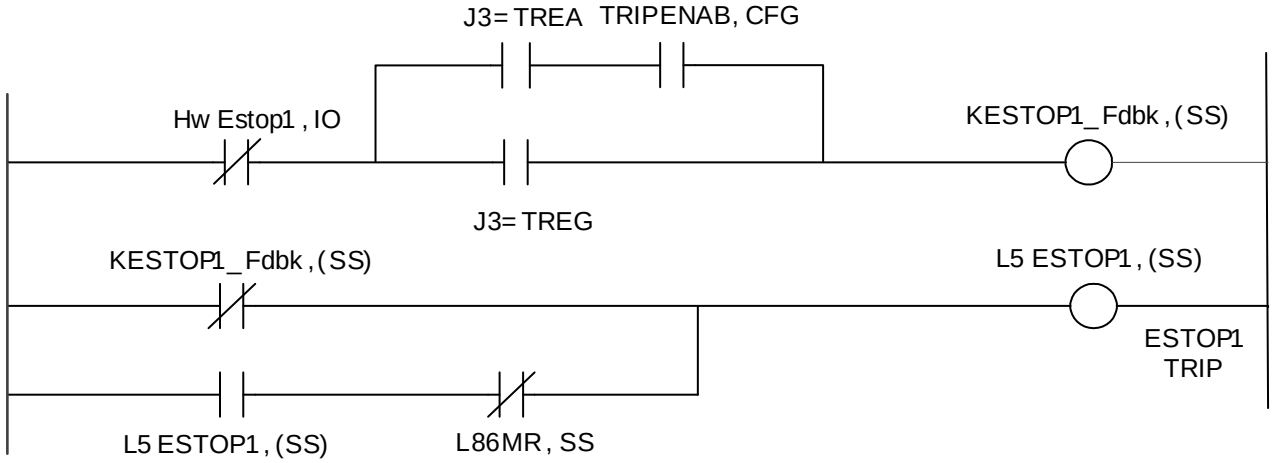
This is another protection function that is in addition to the overspeed protection. LP Shaft Locked Detection generates a signal if the first pulse rate signal is above minimum speed, and the second pulse rate signal is still at zero.



LP Shaft Locked Detection

7.1.3.8 E-Stop

The I/O pack monitors the E-Stop trip signal that is present on the TREG or TREA terminal boards and uses it to cross trip the main control in the event E-Stop is invoked. It is also used within the pack logic as part of the trip relay output command. The relays are not required to close if the E-Stop signal is present. The main control counterpart is also present. If the main control votes to trip, it can also cross-trip the corresponding I/O pack.

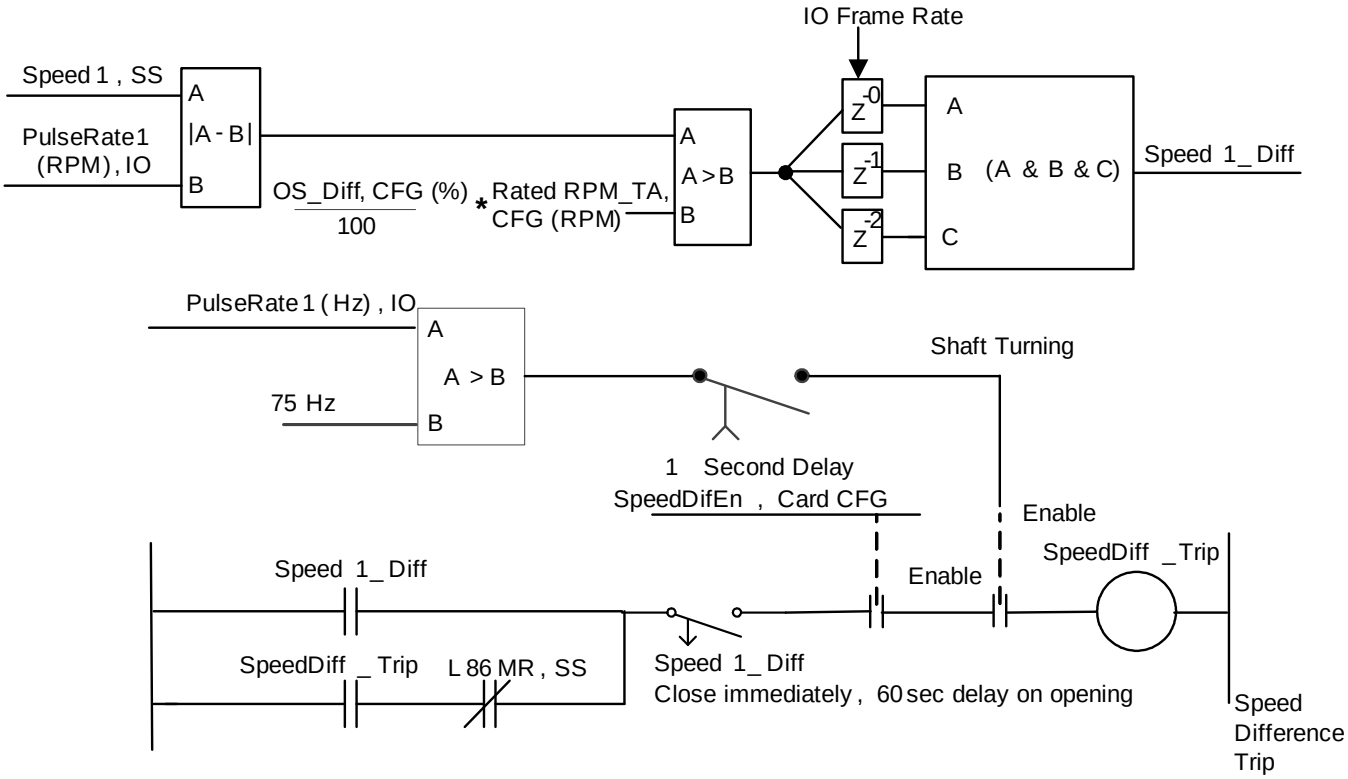


Contact Input E-Stop

Note There are several inversions in the hardware signal path, but the end result is that KESTOP#_Fdbk is only a 1 when E-Stop is energized. Therefore, 1 = OK. The TREL and TRES terminal boards do not have E-Stop capability because it is on the primary trip boards TRPL and TRPS.

7.1.3.9 Speed Difference Detection

There should never be a reason why the speed calculated by the I/O pack is significantly different from the speed calculated by the main control. Speed difference detection looks at the difference in magnitude between pulse rate 1 from both the pack and the main control. If the difference is greater than the set threshold for three successive samples, a *SpeedDifTrip* is latched. If the main control recovers for 60 seconds, the trip is removed. This allows the main control to recover with subsequent re-arming of the backup protection.



When configured for dual controller, additional logic is added so that separate speed inputs from the two controllers come into the I/O pack. This trip logic acts as if both controllers have a speed error, but continues to run if one controller has a valid speed signal.

7.1.3.10 Maximum Speed Hold

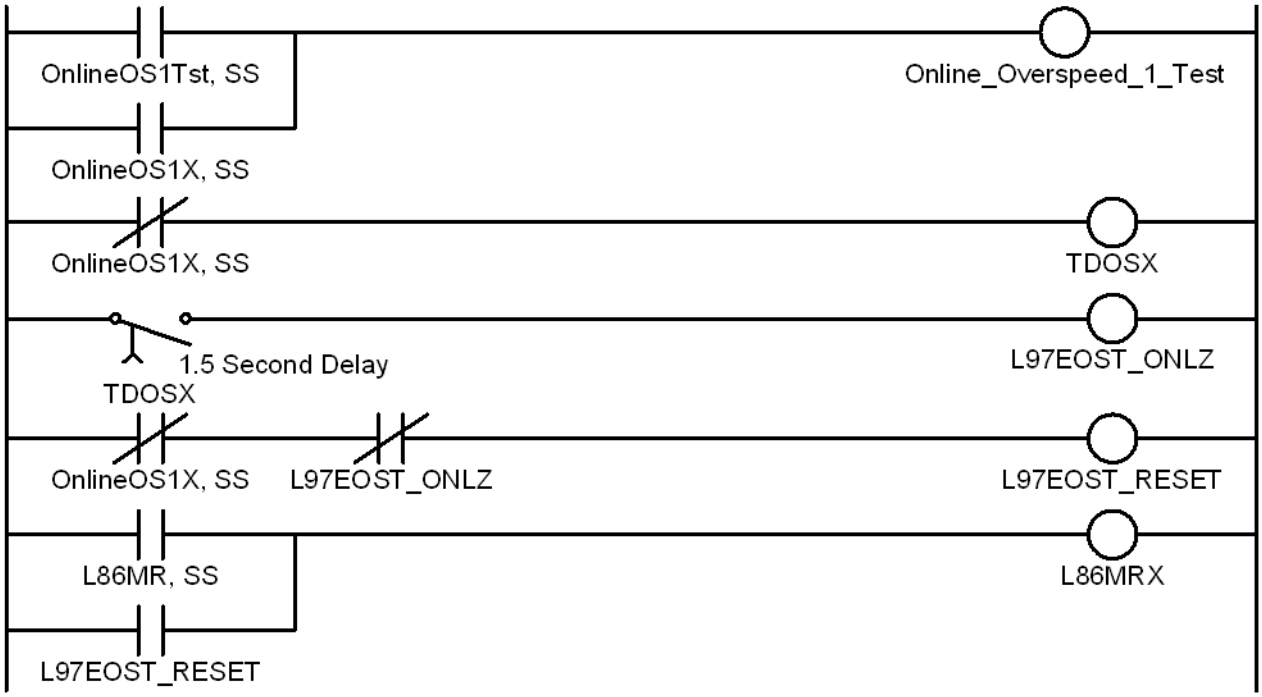
The I/O pack provides a maximum speed hold function that resets when:

- Using the command PR_Max_RST (from signal space)
- PR1_Zero changes to false when the shaft first starts turning

Output values are PR1_Max, PR2_Max, and PR3_Max. These signals are used to determine the maximum speed obtained while running or after stopping a turbine.

7.1.3.11 Overspeed Test Logic, Steam Turbine

The signal OnLineOS1Tst is used for PulseRate1, OnLineOS2Tst is used for PulseRate2, and OnLineOS3Tst is used for PulseRate3. In the following figure, there is another signal, Online OS1X, which initiates an online overspeed test for PulseRate1. This signal also creates a 1.5 second reset pulse when removed.



Online Overspeed Test Logic

Note If the K4CL relay is enabled during an online Overspeed test, use the OnlineOS1X option and not the OnlineOS1Tst. This will avoid an unwanted K4CL activation.

7.1.3.12 Speed State Boolean Values

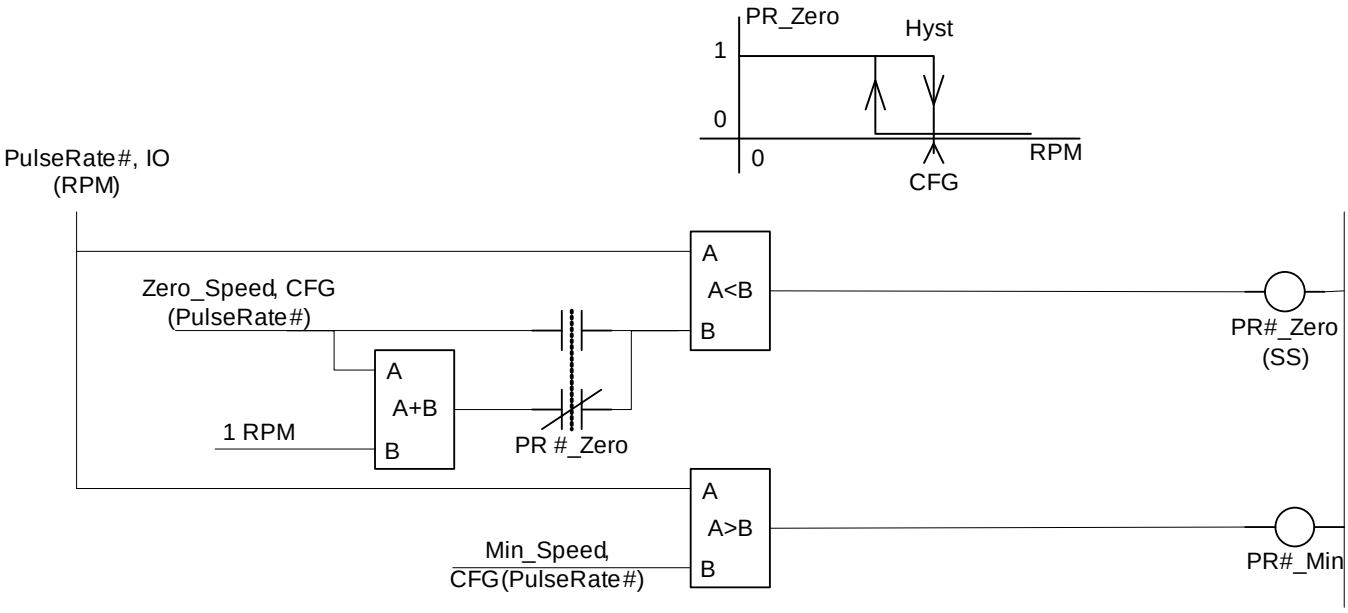
The I/O pack has detection for zero speed from a set point with 1 RPM hysteresis. The I/O pack calculates a minimum speed signal from a set point. The rate of change of speed from a set point is calculated resulting in a selectable acceleration trip. A deceleration trip is then determined from a fixed 100% / second rate.

7.1.3.13 Shaft Speed Accel, Decel and Zero

The I/O pack has detection for zero speed from a set point with 1 RPM hysteresis. The I/O pack calculates a minimum speed signal from a set point. The rate of change of speed from a set point is calculated, resulting in a selectable acceleration trip. A deceleration trip is then determined from a fixed 100% / second rate.

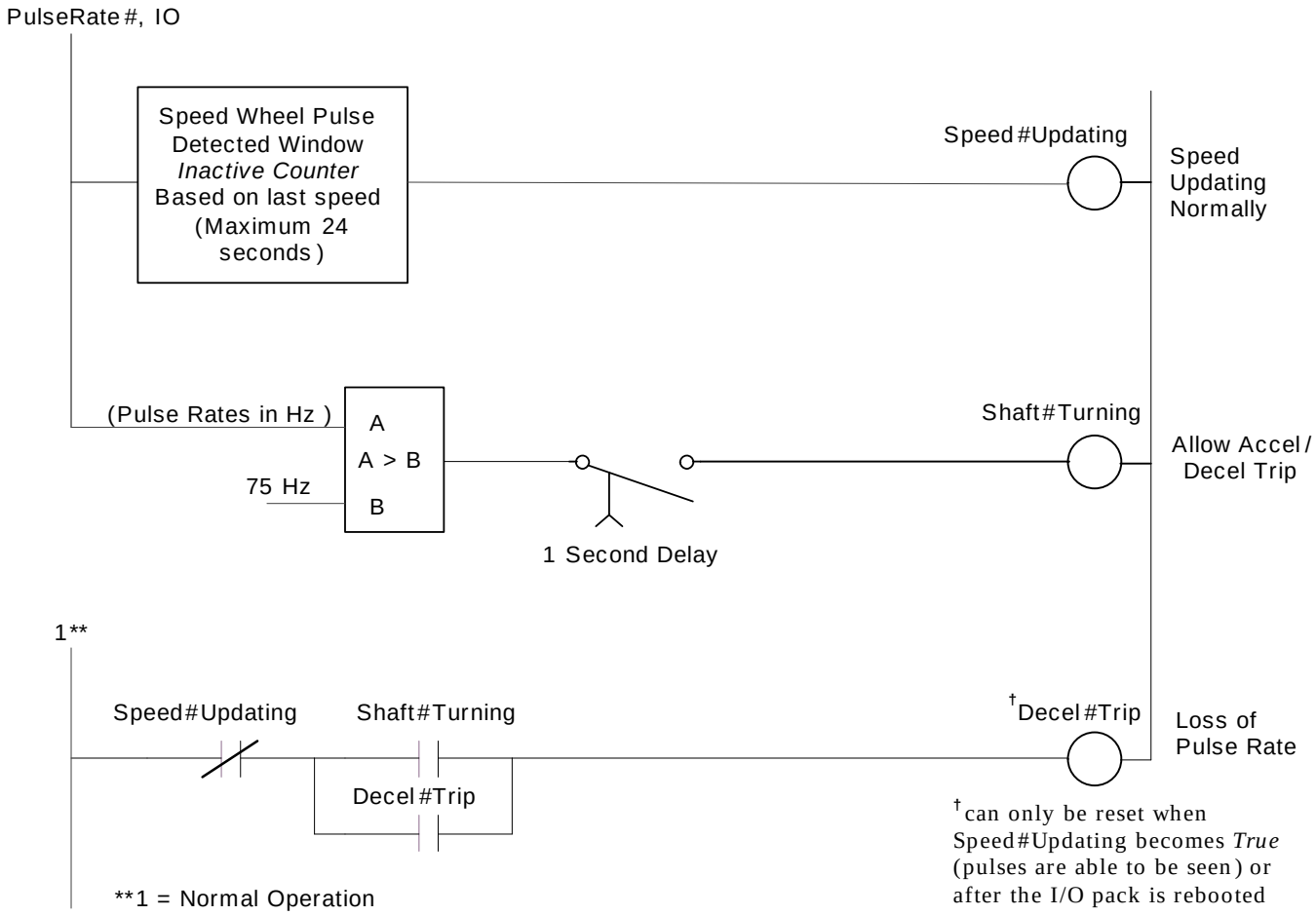
The acceleration for a given pulse rate (*PR#_Accel*) is calculated by computing two adjacent shaft speeds over a period of AccelCalType ms each by computing change in pulse counts, and then computing the difference in these speeds divided by AccelCalType ms to get the acceleration of the shaft.

In the following figures, pulse rate variables are displayed using a # symbol. Replace the # with 1 for HP, 2 for LP, or 3 for IP. This figure is the same for PulseRate1, 2, and 3. Simply replace the 1 with a 2 or 3 to get the signal name. The contact, PR#_ Min, in the Acc1_Trip is only present for PR2 (PR2_Min) and PR3 (PR3_Min). It is not used for PR1.

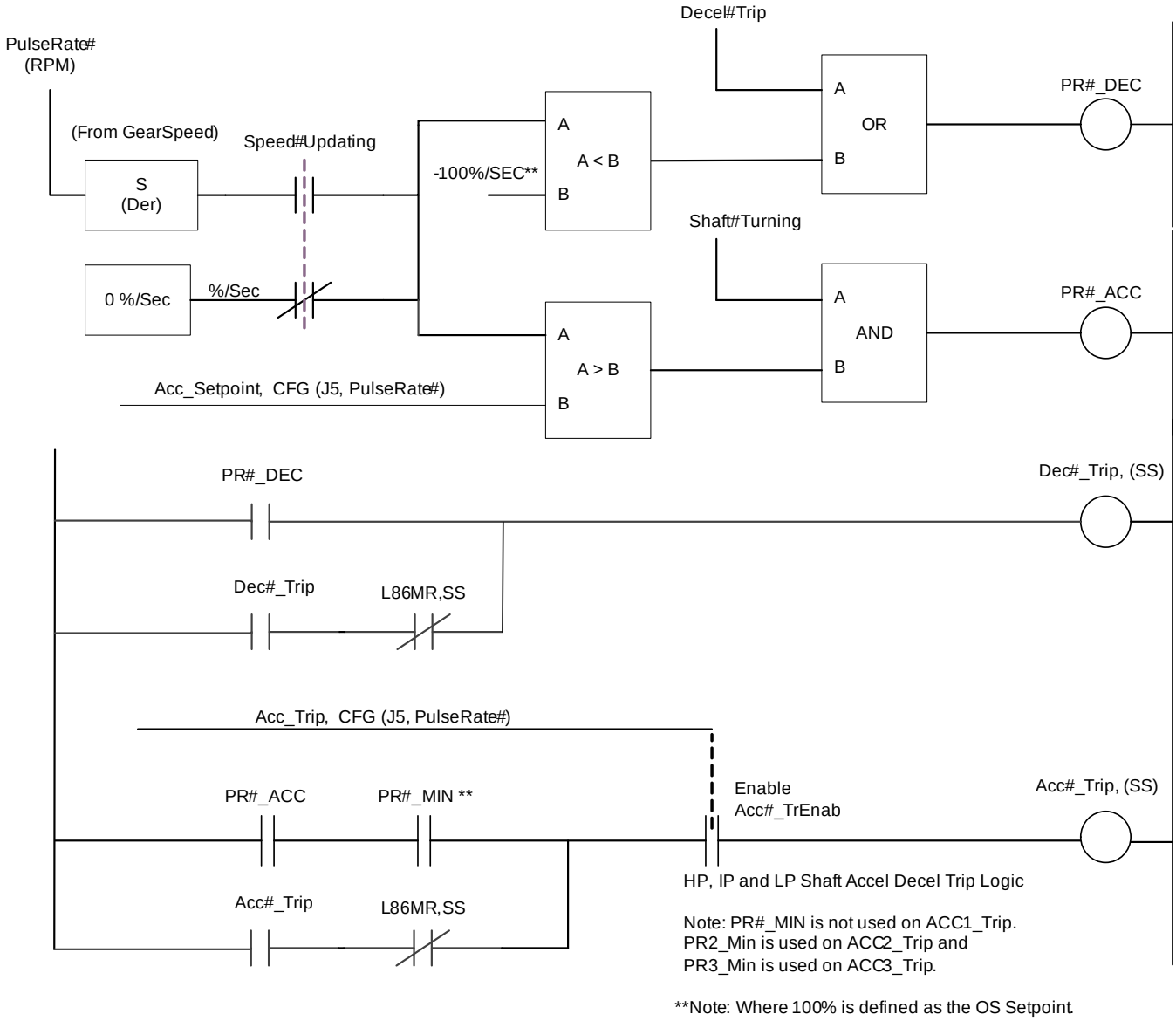


Speed State Boolean Values

The pulse rate inputs have special detection for loss of signal, and special filtering to remove input noise from nearly stationary shaft speeds.



Pulse Rate Conditioning



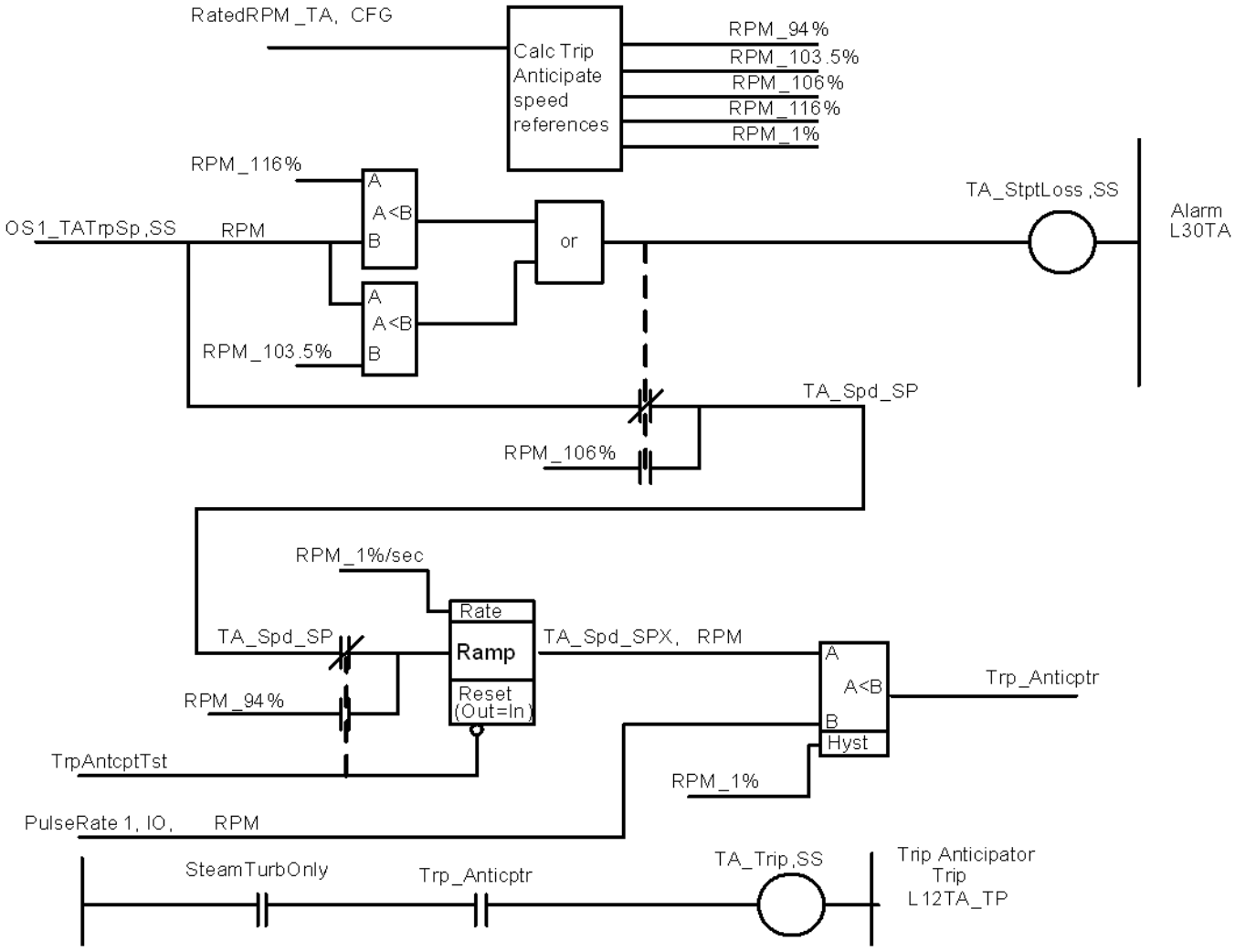
Shaft Speed Accel, Decel and Zero

7.1.3.14 Trip Anticipate Function

Steam turbine applications provide a speed trip that uses a live set point from signal space. This overspeed trip is vigorously changed as a function of turbine load. This function does the following:

- Input set point is OS1_TATrpSp from signal space. Input rated RPM is specified by RatedRPM_TA as part of the I/O pack configuration. Function test request input is TrpAntcptTst from signal space.
- If (OS1_TATrpSP is < 103.5% OR > 116% of RatedRPM_TA) then TA_Spd_Sp (the local set point value) = 106% of RatedRPM_TA and TA_StptLoss (Signal space) is true and alarm L30TA is declared. Otherwise, TA_Spd_Sp = OS1_ TATrpSP.
- If TrpAntcptTst is true, decrease the current value of TA_Spd_Sp by 1RPM / second. Set the minimum value of RatedRPM_TA to 94%. If TrpAntcptTst is false, the value of TA_Spd_Sp from above is immediately used.
- If PulseRate1 (Speed input 1 from the pulse rate input) > TA_Spd_Sp the internal value Trp_Anticptr is set properly.
- If the I/O pack is configured for steam turbine application (internal value SteamTurbOnly), then TA_Trip (signal space) equals the value of Trp_Anticptr.

Note The I/O pack mounted on a TREA does not toggle the relays for trip anticipate function.



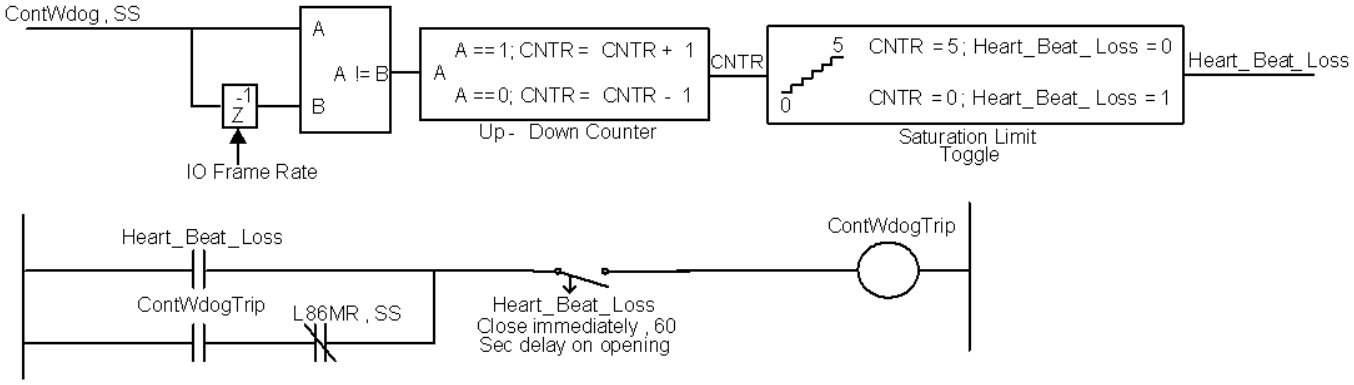
7.1.3.15 Solenoid Voltage / Power Sense

The I/O pack provides three comparator voltage inputs used to monitor solenoid power or solenoid voltage depending on the trip card that is connected. SOL1_Vfdbk (SS), SOL2_Vfdbk (SS), and SOL3_Vfdbk (SS) are generated from the input signals.

7.1.3.16 Main Control Watchdog

A standard control watchdog function is provided by the I/O pack. In this function, a value from a Device Heartbeat (DEVICE_HB) block is passed from the main controller to the I/O pack each data frame. If the I/O pack stops detecting the value from the main controller, a counter is incremented and, after five data frames, leads to a trip. If the main controller recovers for 60 seconds, the trip is removed, allowing for the recovery of the main controller with subsequent re-arming of the backup protection. The recovery function is provided for typical activities such as cycling power on a controller to perform maintenance.

While the controller is offline, the I/O pack associated with that controller will vote to trip. When the controller returns to operation, the I/O pack will remove the vote to trip. The watchdog offers monitoring of two main controllers in the event both Ethernet ports are connected. When configured for two controllers, having one controller active is sufficient to prevent a trip.



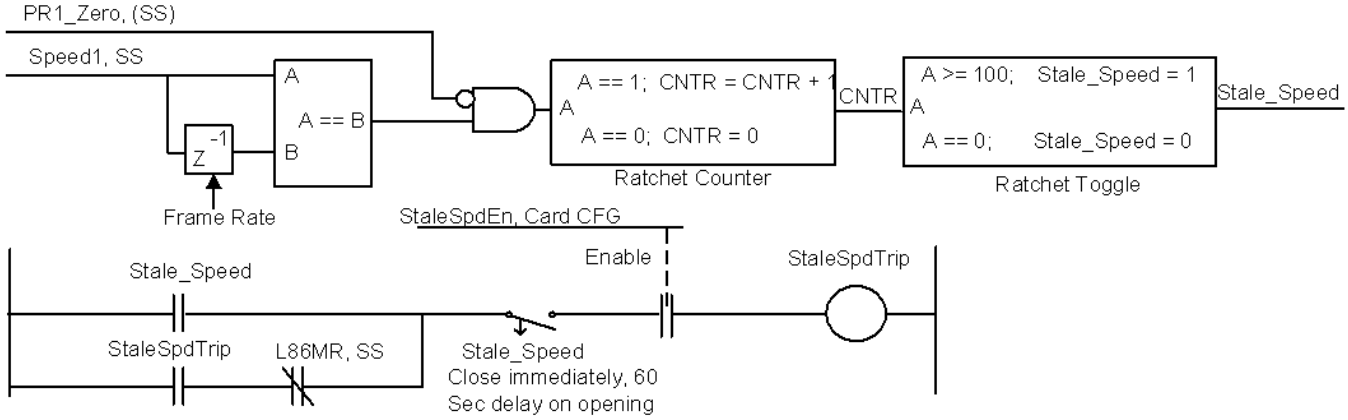
7.1.3.17 Stale Speed Detection

The I/O pack provides an additional main control watchdog function that is based on a live speed signal. The protection works as follows: If the pack PulseRate1 is determined to be zero speed the protection is turned off. If above zero speed, the pack looks at the value of Speed1 from the main control. If the most recent Speed1 value exactly matches the Speed1 value from the last data frame then a counter is incremented. If the counter reaches a threshold then a stale speed trip is declared and latched. If speeds are different the counter is cleared.

Attention

Although Speed_1, SS is available as a connected variable, it should not be forced. It can cause the protection to trip the system if enabled.

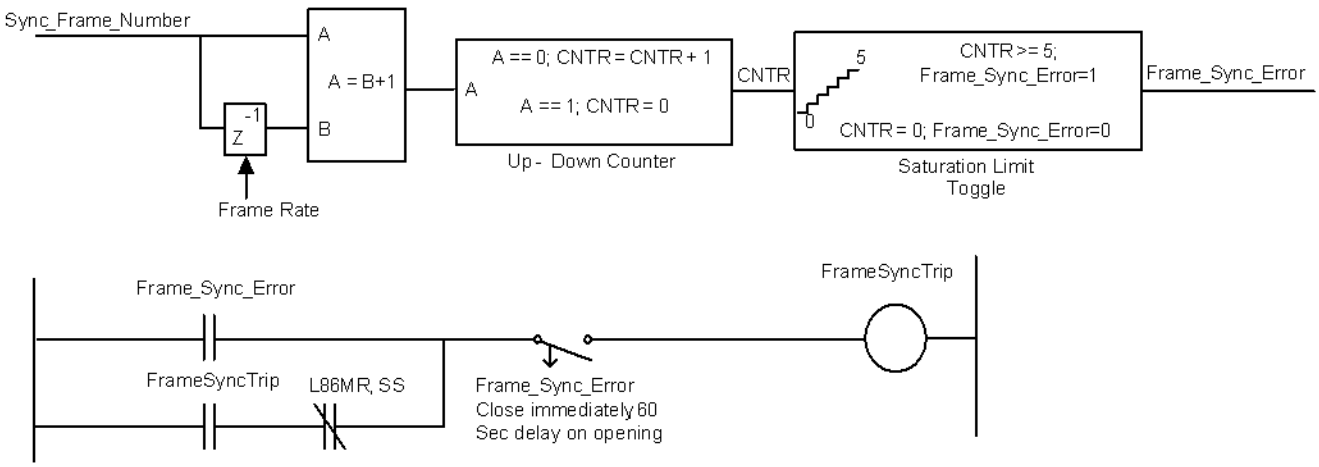
This protection is based on the knowledge that a live speed signal always *dithers* or moves some small amount. If the speed values being read by PPRO from the controller are not changing (dithering), there is loss of speed signal integrity from the controller. If the main control recovers for 60 seconds, the trip is removed allowing for the recovery of the main control with subsequent re-arming of the backup protection. The protection offers monitoring of two main controls in the event both Ethernet ports are connected. When configured for two controls, having one control satisfy the test is sufficient to prevent a trip.



7.1.3.18 Main Control Ethernet Monitor

The main control provides time synchronization across the distributed control elements. The time synchronization is tied tightly into the time at which traffic occurs on a given controller's IONet. The I/O pack provides monitoring of this service to ensure it is working correctly. Gross errors in time synchronization are detected by the pack through a number of different means, and if problems persist, the I/O pack will vote to trip. Once the trip is latched, if the problem goes away for 60 seconds the trip shall be reset (this assumes the control recovers from the problem and is back on line). The monitor will offer monitoring of two main controls in the event both Ethernet ports are connected. When configured for two controls, having one control sequencing correctly is sufficient to prevent a trip.

In the following diagram, the detection has been simplified to display monitoring of an Ethernet frame number as the means for determining a problem is present.

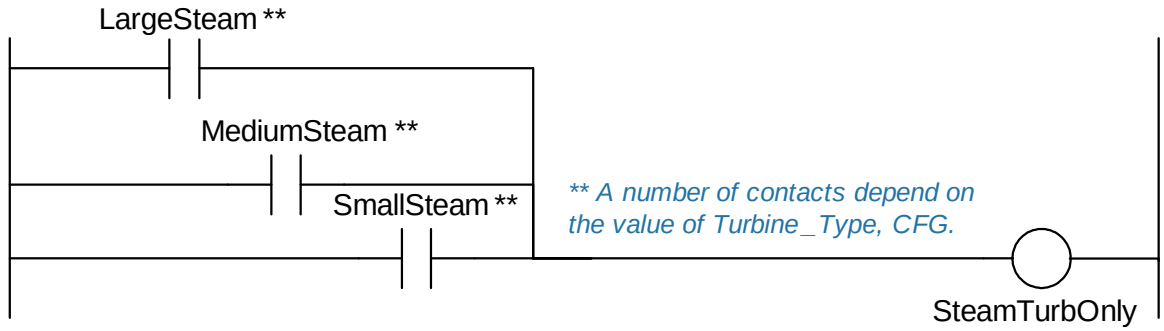


Sync Frame Count Monitor

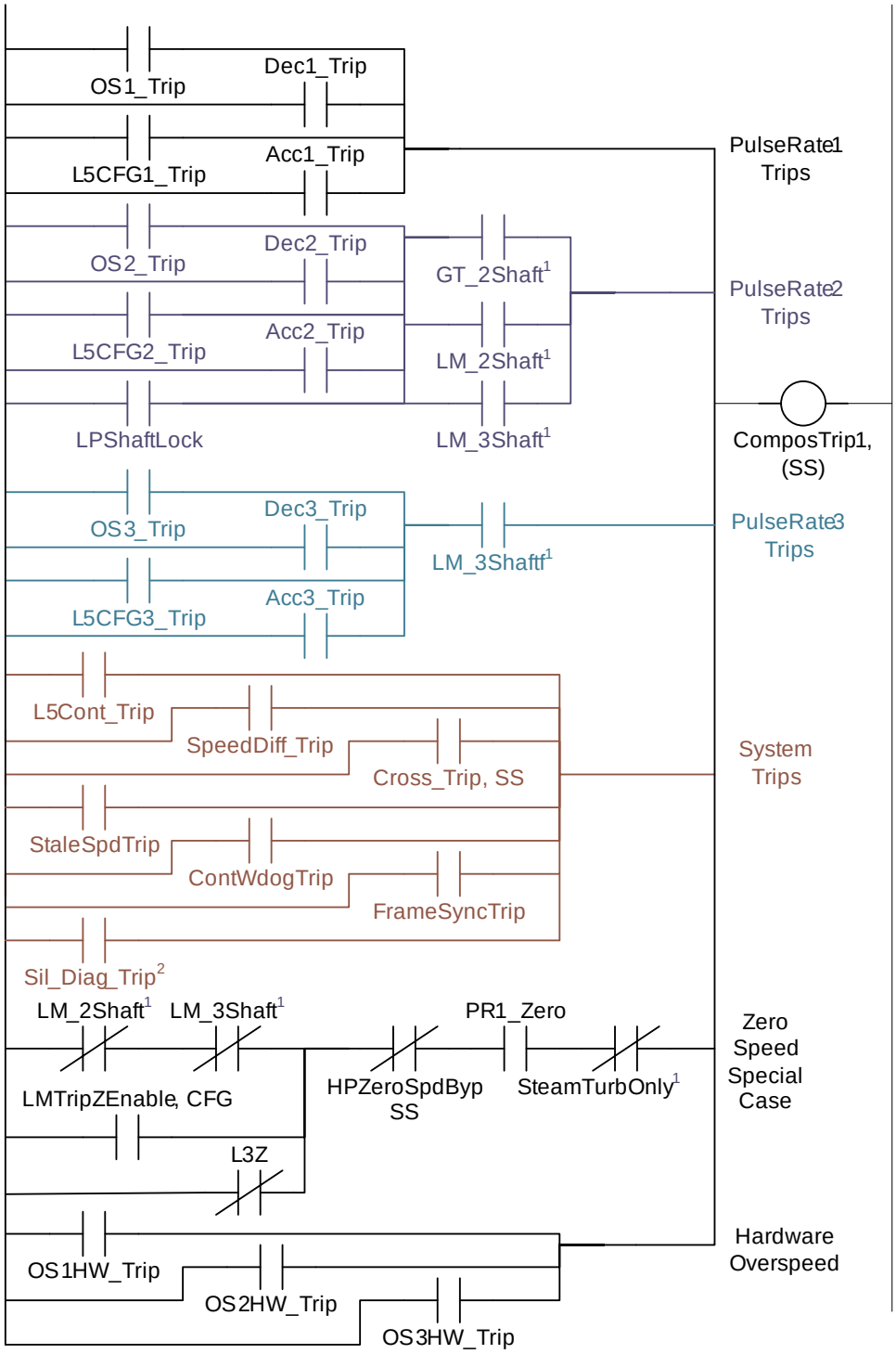
7.1.3.19 Trip Signal Logic

The different trip signals are combined into a composite signal that is used in the relay output logic. The following figure specifies how the signals are combined. This function is partitioned between firmware and programmable logic. The path to trip through hardware overspeed is done completely in hardware so that a firmware malfunction cannot defeat the protection. The same is true of the contact input trip signals when they are configured for direct trip.

There are differences between steam turbine protection and other protection. A composite signal SteamTurbOnly is created for ease of use:



Steam Turbine Trip Signals



Notes: [1] CFG values.

[2] This trip is generated if a *PulseRate* signal is broken (such as in the case of no signal) and *SilMode* is set to enabled, or if a hardware issue is detected regardless of *SilMode*. There will be an accompanying diagnostic generated to designate the actual cause of the trip

Trip Combine - All Signals (SS) unless Marked

7.1.3.20 Watchdog Trip Function

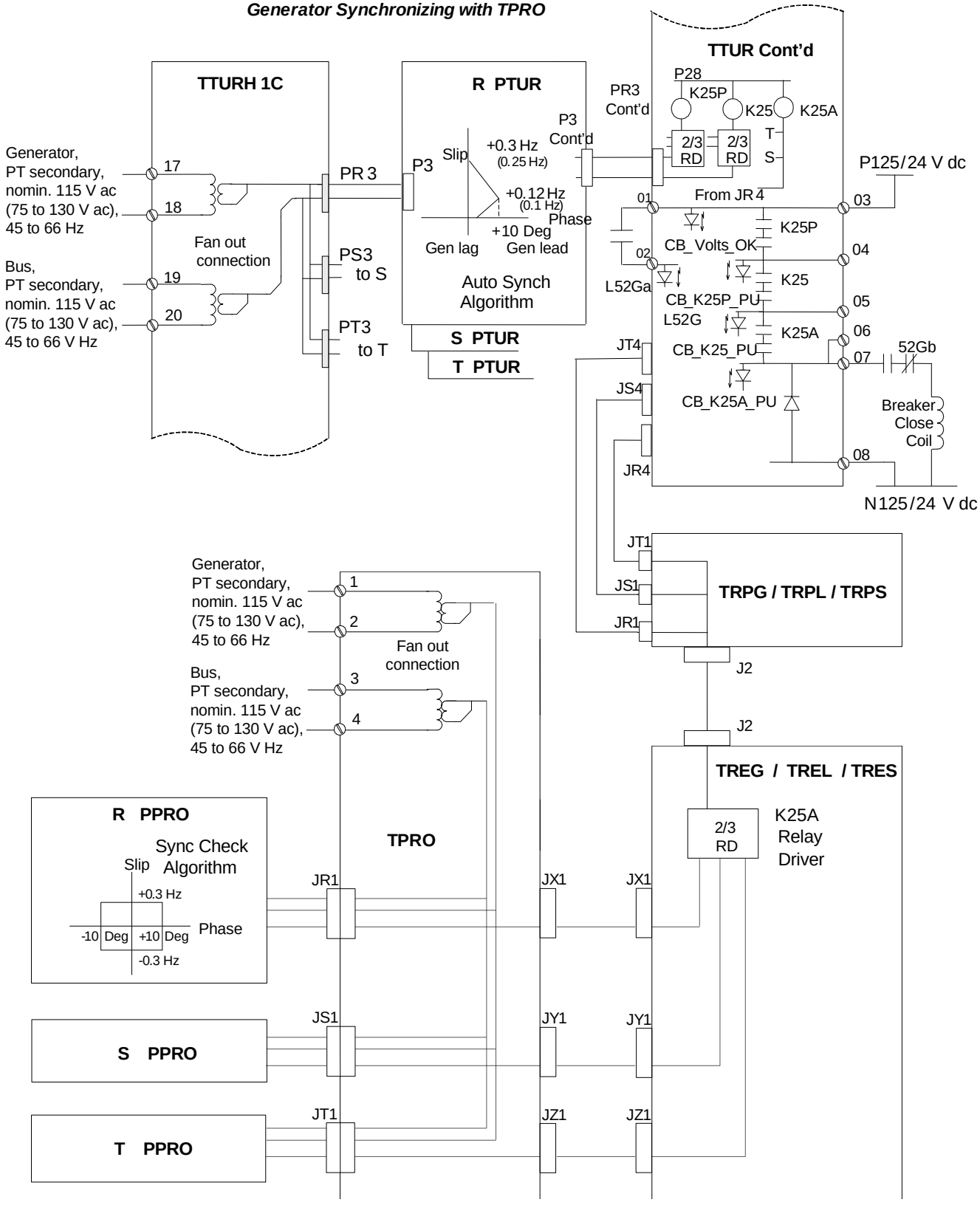
Hardware in the I/O pack monitors local firmware operation, providing a watchdog trip function if the firmware malfunctions. The operation of this watchdog does not display in the normal sequencing figures. The I/O pack hardware is designed to be in a fail-safe or trip mode if it is not properly configured and operating. This means that with power off, while starting up, when in a hardware reset, or otherwise not online, the I/O pack will vote to trip. If the I/O pack watchdog acts, it resets the hardware thereby generating a vote to trip.

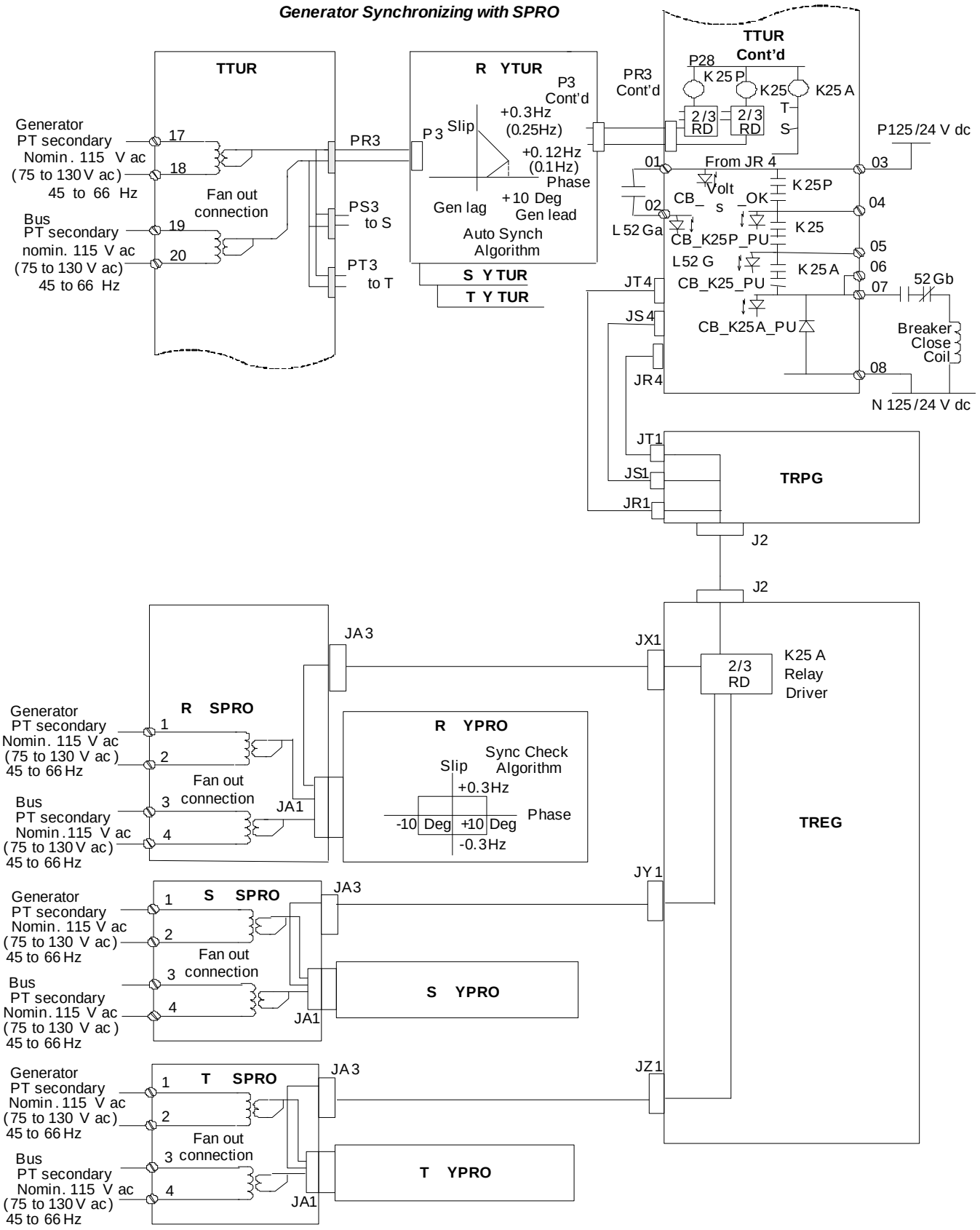
The processor board used inside the I/O pack has hardware features that allow it to differentiate between a reset caused by the watchdog hardware and a reset caused by cycling of power. This information is available from the pack after it restarts. In the event that an I/O pack votes to trip due to a reset, it is then possible to determine if a watchdog reset or a cycling of control power caused the event.

7.1.3.21 Backup Synchronizing Check

The Mark VIeS YPRO or Mark VIe PPRO provides two PT inputs and performs a backup synchronizing check. The TPRO has fanned PT inputs. The SPRO does not use fanned PT inputs because there are three direct PT paths.

Generator Synchronizing with TPRO



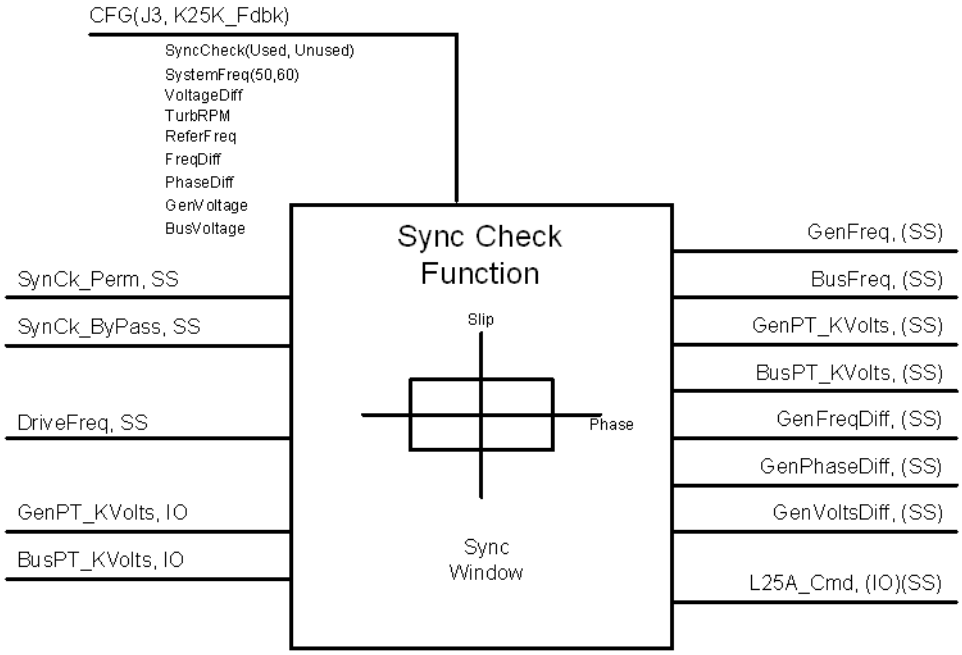

Generator Synchronizing with SPRO
TTUR
Generator PT secondary Nomin. 115 V ac (75 to 130 V ac) 45 to 66 Hz
17
18
Fan out connection
Bus PT secondary nomin. 115 V ac (75 to 130 V ac) 45 to 66 Hz
19
20
PR3
PS3 to S
PT3 to T
R YTUR
P3 Cont'd
P3 Slip
+0.3Hz (0.25Hz)
+0.12Hz (0.1Hz)
Phase
Gen lag
+10 Deg
Gen lead
Auto Synch Algorithm
S Y TUR
T Y TUR
TTUR Cont'd
PR3 Cont'd
P28
K25P
K25
K25A
2/3 RD
2/3 RD
T
S
P125/24 V dc
From JR4
01
03
Volt
K25P
CB_s_OK
02
04
L52Ga
K25
CB_K25P_PU
05
L52G
K25A
06
CB_K25_PU
JT4
07
52Gb
JS4
CB_K25A_PU
Breaker Close Coil
08
JR4
N 125/24 V dc
JT1
JS1
JR1
TRPG
J2
J2
JA3
JX1
2/3 RD
K25A Relay Driver
R SPRO
Generator PT secondary Nomin. 115 V ac (75 to 130 V ac) 45 to 66 Hz
1
2
Fan out connection
Bus PT secondary Nomin. 115 V ac (75 to 130 V ac) 45 to 66 Hz
3
4
JA1
R YPRO
Slip
Sync Check Algorithm
+0.3Hz
-10 Deg
+10 Deg
Phase
-0.3Hz
TREG
JY1
S SPRO
JA3
S YPRO
JA1
JZ1
T SPRO
JA3
T YPRO
JA1

7.1.3.22 K25A Sync Check Function

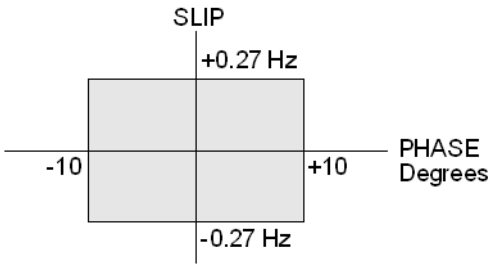
The K25A sync check function is based on phase lock loop techniques. The PPRO or YPRO performs the calculations for this function with interfaces to the breaker close circuit located on the TTUR board (not TPRO or SPRO). Its basic function is to monitor two Potential Transformer (PT) inputs, and to calculate generator and bus voltage amplitudes and frequencies, phase, and slip.

When it is armed (enabled) from the application code, and when the calculations determine that the input variables are within the requirements, the relay K25A will be energized. The above limits are configurable. The algorithm uses the phase lock loop technique to derive the above input variables, and has a bypass function to provide dead bus closures. The window in this algorithm is the current window, not the projected window (as used on the auto sync function), therefore it does not include anticipation. Limit checks are performed against adjustable constants as follows:

- Generator under-voltage
- Bus under-voltage
- Voltage error
- Frequency error (slip), with a maximum recommended value of 0.5 Hz, typically set to 0.27 Hz
- Phase error with a maximum rotational value of 30°, typically set to 10°.

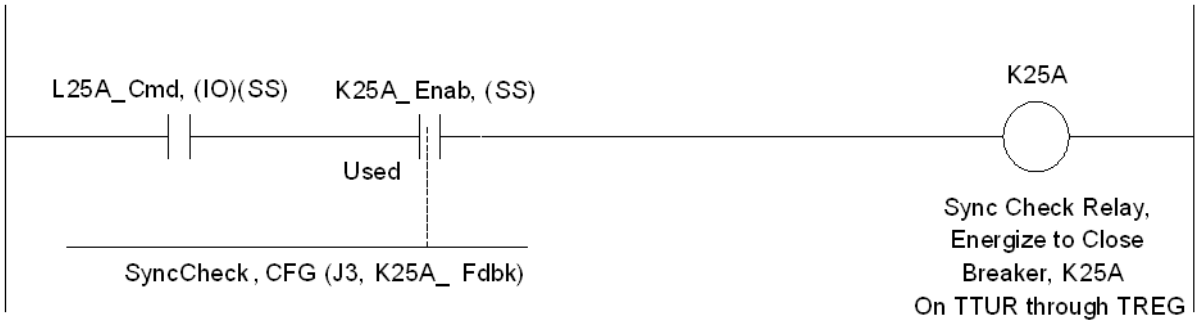


The sync check arms logic to enable the function and provides bypass logic for dead bus closure. The following sync window is based on typical settings.



Typical Sync Window

The PPRO or YPRO provides a command to monitor feedback for the K25A sync relay and K25A coil. The feedback is named K25A_Fdbk, (SS).



Sync Check and K25A Sync Relay Command

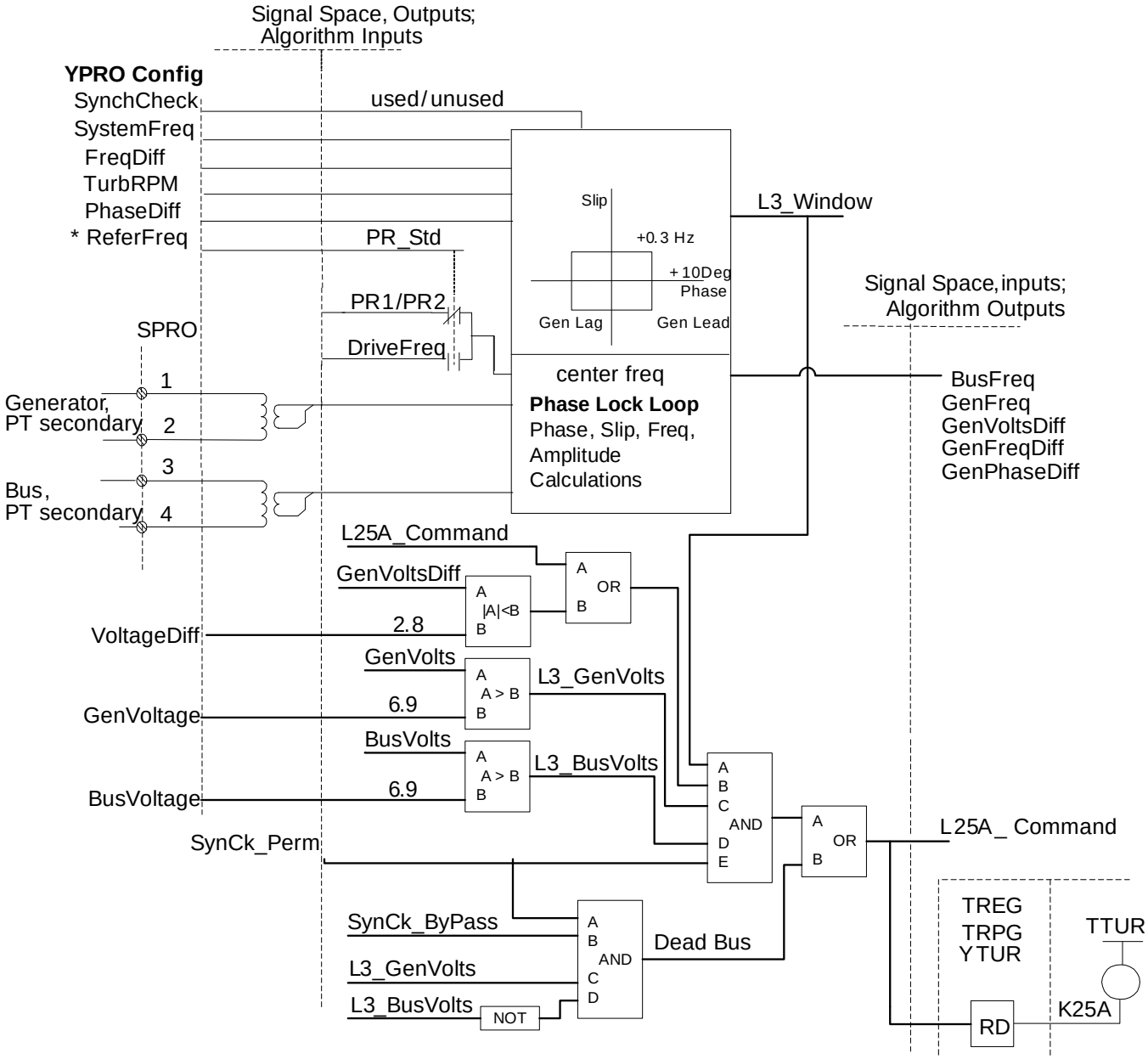
The Sync Check will allow the breaker to close with negative slip. The window is configurable for phase and slip.

The following diagnostics relating to the auto sync function are generated by the PPRO or YPRO:

- K25A Relay (sync check) Driver mismatch requested state. This means the PPRO or YPRO cannot establish a current path to the TREx terminal board.
- K25A Relay (sync check) Coil trouble, cabling to P28 V on TTUR. This means the K25A relay is not functional; it could be due to an open circuit between the TREx and the TTUR terminal boards or to a missing P28 V source on the TTUR terminal board.

7.1.3.23 K25A Relay Algorithm

The following figure displays the logic for K25A Relay from the Mark VIeS YPRO, which is the same as from the Mark VIe PPRO.

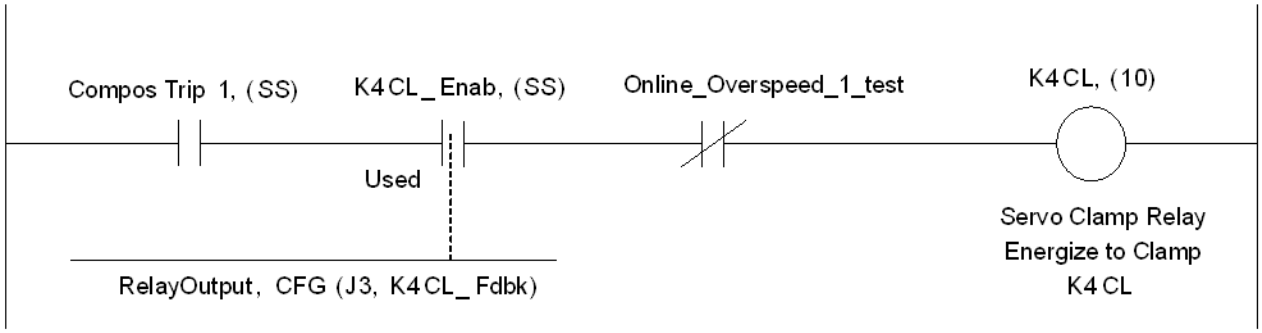


Note **ReferFreq* is a configuration parameter, used to make a selection of the variable that is used to establish the center frequency of the *Phase Lock Loop*. It allows a choice between:

- *PR_Std*
  - Using PulseRate1 speed input on a single shaft applications
  - Using PulseRate2 on all multiple shaft applications
- *SgSpace* uses DriveFreq (the generator frequency in Hz) from signal space (application code). SgSpace is used when PR_Std is not applicable.

7.1.3.24 Servo Suicide Relay Command

The I/O pack provides a command to a servo suicide relay, and provides coil-monitoring feedback named K4CL_Fdbk, (SS). This signal is typically used in a simplex control of a gas turbine system where it is highly desirable for the pack emergency protection to have a hardware path to close the fuel valves. It is also used in simplex steam turbines to close the steam valves.



Servo Suicide Relay Command

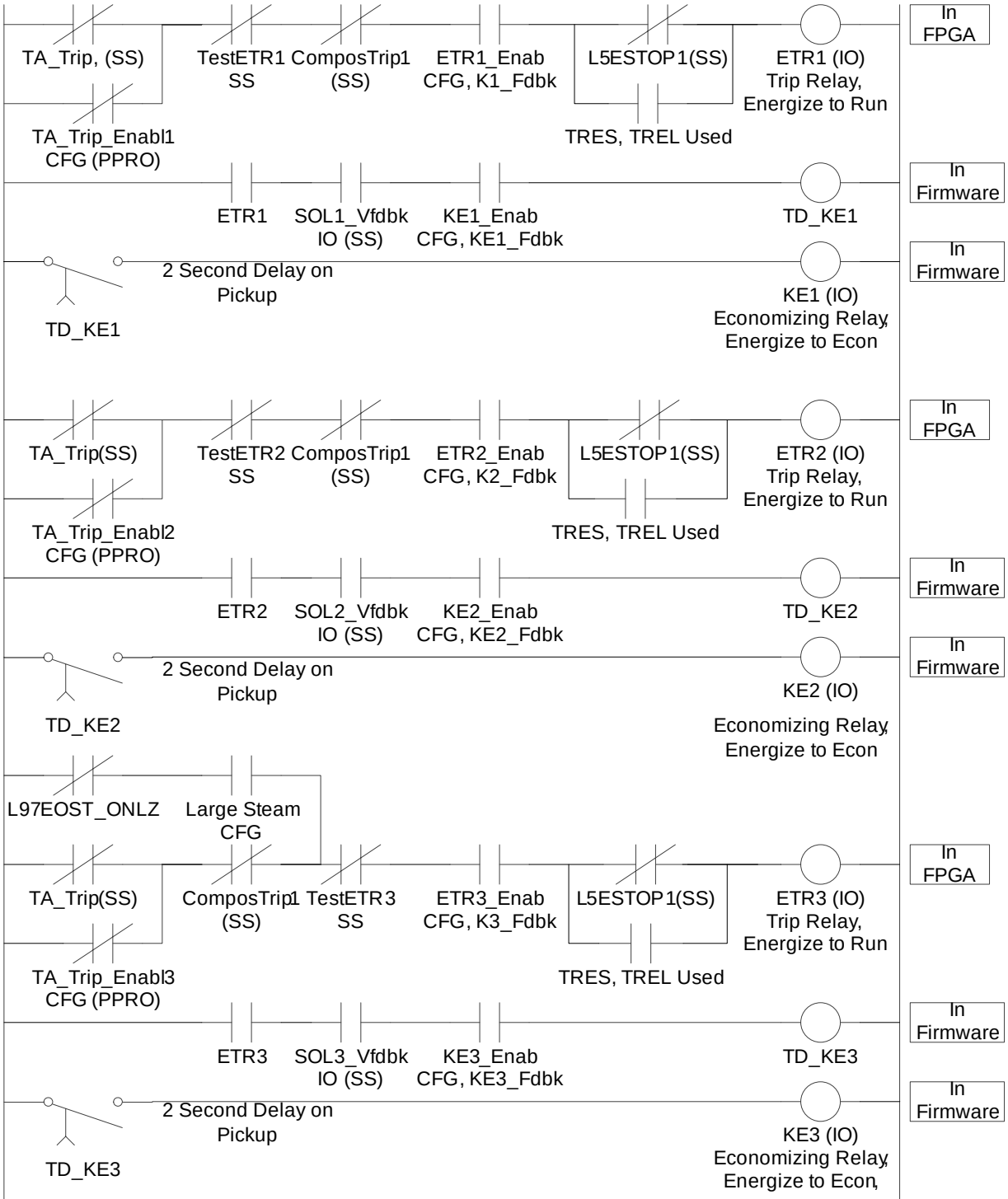
Note If the K4CL relay is enabled during an online Overspeed test, use the OnlineOS1X option and not the OnlineOS1Tst. This will avoid an unwanted K4CL activation.

7.1.3.25 Trip and Economizing Relay Outputs

The I/O pack provides drivers for three emergency trip relay commands, and provides monitoring for three status feedback signals. Trip is a combination of firmware trip and direct trip implemented in programmable logic. The pack contains drivers for three economizing relay commands and monitoring for three status feedback signals. Economizing relays are used when it is desirable to introduce some series resistance in a solenoid coil path to reduce current once the solenoid is picked up.

Note YPROs or PPROs mounted on TREA terminal boards have TA_Trip_Enab# set by default to Disable and this parameter is not configurable.

The reset signal applied to this function is not edge triggered. A continuously applied reset can result in output cycling in the presence of an intermittent trip signal. The duration of the reset should only be sufficient to allow the reset to complete and should not be maintained. Logic for the economizing relay drivers is a time-delayed copy of the emergency trip relays as displayed in the following figure.



Trip and Economizing Relay Outputs

7.1.4 Specifications

Item	PPRO Specification
Speed Input Quantity	Three input signals provided
Speed input Range	Pulse rate frequency range 2 Hz to 20 kHz
Speed Input Accuracy	Pulse rate accuracy 0.05% of reading
Speed Input Sensitivity Speed input sensitivity is such that turning gear speed may be observed on a typical turbine application.	Required peak-peak (p-p) voltage rises as a function of frequency: 2 Hz requires 27 mV p-p (TREA, SPRO, TPRO) 20 kHz requires 294 mV p-p (TREA) 20 kHz requires 276 mV p-p (SPRO, TPRO)
Generator and Bus Voltage Inputs	Input voltage range 75 to 127 V rms. Loading less than 3 VA. Frequency accuracy 0.05% over 45 to 66 Hz range.
Frame Rate	100 Hz maximum
Pulse Duration Limitation	Trip contact input can only be detected if the pulse contact is greater than 8 ms.
Size	8.26 cm high x 4.19 cm wide (3.25 in x 1.65 in x 4.78 in)
Technology	Surface-mount
† Ambient rating for enclosure design	PPROS1B is rated from -40 to 70ºC (-40 to 158 ºF) PPROH1A is rated from -30 to 65ºC (-22 to 149 ºF) † Refer to GEH-6721_Vol_I, the chapter *Technical Regulations, Standards, and Environments.*
Vibration	
Seismic	Universal Building Code (UBC) – Seismic Code section 2312 Zone 4 with operation without trip
Shipping (by road)	Bellcore GR-63-CORE Issue 1, 1995 0.5 g, 5-100 Hz, 10 min. per octave, 1 sweep/axis x 3 axes, ~ 42 min./axis 3 shocks of 15 g, 2 ms impulse each repeated for all axes
Operating at site	1.0 g horizontal. 0.5 g vertical at 15 to 120 Hz IEC 60721-3-2

Agency Approvals

Type	Standards
Safety	UL 508A Safety Standard Industrial Control Equipment CSA 22.2 No. 14 Industrial Control Equipment EN 61010-1 Safety of Electrical Equipment, Industrial Machines (Low Voltage Directive)
Printed Wire Board Assemblies	UL 796 Printed Circuit Boards UL recognized Board manufacturer ANSI IPC guidelines ANSI IPC/EIA guidelines
Electromagnetic Compatibility (EMC)	EN 61000-4-2 Electrostatic Discharge Susceptibility EN 6100 4-3 (ENV 50140) Radiated RF Immunity EN 61000-6-2 Generic Immunity Industrial Environment EN 61000-4-4 Electrical Fast Transient Susceptibility EN 61000-4-5 Surge Immunity EN 61000-4-6 Conducted RF Immunity EN 55011 Radiated and Conducted RF Emissions ANSI/IEEE C37.90.1 Surge

7.1.5 Diagnostics

The I/O pack performs the following self-diagnostic tests:

- A power-up self-test that includes checks of RAM, flash memory, Ethernet ports, and most of the processor board hardware
- Continuous monitoring of the internal power supplies for correct operation
- A check of the analog feedback currents
- A comparison between the commanded state of each relay drive and the feedback from the commanded output circuit
- A check of the electronic ID information from the terminal board, acquisition board, and processor board to confirm that the hardware set matches, followed by a check that the application code loaded from flash memory is correct for the hardware set

Details of the individual diagnostics are available from the ToolboxST application. The diagnostic signals can be individually latched, and then reset with the RESET_DIA signal if they go health.

7.1.5.1 PPRO Trip Status

During normal I/O pack operation, all six trip application LEDs display green. An additional feature, rotating LEDs, can be configured for the I/O pack. Using this feature, only one LED is turned on at a time, and walked up and down the six LEDs creating a synchronized motion. The walking is regulated by the controller IONet, and synchronized across a set of three I/O packs. This provides a quick visual indication of the system time synchronization status. There are six LEDs on the front left side of the I/O pack to indicate trip status. All six LEDs stay off until the I/O pack is completely online.

RUN is green any time the I/O pack has energized the emergency trip relays. RUN turns red any time the I/O pack has removed power from the emergency trip relays, voting to trip.

ESTP is green when the ESTOP input (if applicable) is in the run state. ESTP turns red any time ESTOP is invoked to prevent pick up of the emergency trip relays. If the selected trip terminal board does not support ESTOP, then the LED defaults to green.

OSPD turns red any time the I/O pack votes to trip in response to a detected overspeed condition on any of the three speed inputs. OSPD is green when an overspeed condition is not present or latched.

Note WDOG turns green to indicate that the trip status of any of these features has been cleared.

WDOG turns red when any of the following I/O pack trip functions are enabled and active:

- Control Watchdog
- Speed Difference Detection
- Stale Speed Detection
- Frame Sync Monitor

SYNC is green when generator and bus voltage is synchronized and matched in amplitude. SYNC turns red when the I/O pack determines that ac bus and generator bus voltage does not satisfy the synchronization requirements, and synchronization has been requested by the system.

OPT is reserved for options that expand the capabilities of the I/O pack. The default display is green.

7.1.6 Configuration

The following subsections (Parameters, Pulse Rate, PT, K25A, and so forth) define the choices within the tabs of the ToolboxST configuration.

7.1.6.1 Parameters

Parameter	Description	Choices
TurbineType	Turbine Type and Trip Solenoid configuration	Unused, GT_1Shaft, LM_3Shaft, MediumSteam, SmallSteam,GT_2Shaft, Stag_GT_1Sh,Stag_GT_2Sh, LargeSteam, LM_2Shaft
LMTripZEnabl	On LM machine, when no PR on Z,Enable a vote for trip	Disable, Enable
TA_Trp_Enab1	Steam, enable trip anticipate on ETR1	† Disable, Enable
TA_Trp_Enab2	Steam, enable trip anticipate on ETR2	† Disable, Enable
TA_Trp_Enab3	Steam, enable trip anticipate on ETR3	† Disable, Enable
StaleSpdEn	Enable trip on speed from controller freezing	Disable, Enable
SpeedDifEn	Enable trip on speed difference between controller and PPRO	Disable, Enable
DiagSolPwrA	When using TREL/TRES, sol power, bus A, diagnostic enable	Disable, Enable
DiagSolPwrB	When using TREL/TRES, sol power, bus B, diagnostic enable	Disable, Enable
DiagSolPwrC	When using TREL/TRES, sol power, bus C, diagnostic enable	Disable, Enable
RotateLeds	Rotate the status LEDs if all status are OK	Disable, Enable
LedDiags	**Attention** **LedDiags is disabled by default.** When enabled, generates a diagnostic alarm when Trip LEDs are lit. Refer to the section, Diagnostics, *PPRO Trip Status* for more information on LED operation.	Disable, Enable
SilMode	Perform additional SIL diagnostic and trip checks	Disable, Enable
RatedRPM_TA	Rated RPM, used for trip anticipater and for speed diff protection	0 to 20,000
AccelCalType	Select acceleration calculation time (milliseconds)	10 to 100
OS_Diff	Absolute speed difference in percent for trip threshold	0 to 10
RBOS1_Enab	HP Rate-based Overspeed enable	Disable, Enable
‡ RBOS1_AccelSetpt*n*, n=1-5	HP Rate-based Overspeed acceleration setpoint *n*, RPM/s	0 to 20,000
‡ RBOS1_OSSetpt*n*, n= 1-5	HP Rate-based Overspeed setpoint *n*, RPM	0 to 20,000
RBOS2_Enab	LP Rate-based Overspeed enable	Disable, Enable
‡ RBOS2_AccelSetpt*n*, n=1-5	LP Rate-based Overspeed acceleration setpoint *n*, RPM/s	0 to 20,000

Parameter	Description	Choices
‡ RBOS2_OSSetpt*n*, n= 1-5	LP Rate-based Overspeed setpoint *n*, RPM	0 to 20,000
RBOS3_Enab	IP Rate-based Overspeed enable	Disable, Enable
‡ RBOS3_AccelSetpt*n*, n=1-5	IP Rate-based Overspeed acceleration setpoint *n*, RPM/s	0 to 20,000
‡ RBOS3_OSSetpt*n*, n= 1-5	IP Rate-based Overspeed setpoint *n*, RPM	0 to 20,000
† PPROs mounted on TREA terminal boards have TA_Trp_Enab# set by default to Disable and this parameter is not configurable. ‡ RBOS setpoints have restrictions in their relative values. Refer to the section *RBOS Parameter Restrictions* for further details.		

7.1.6.2 RBOS Parameter Restrictions

The following restrictions apply to the relative values of RBOS setpoints (within a given shaft):

1. RBOS#_AccelSetpts must increase in value by at least 0.1 RPM/s (RBOS1_AccelSetpt2 must be 0.1 RPM/s or greater than RBOS1_AccelSetpt1). This prevents an infinite slope calculation in the overspeed setpoint profile.
2. RBOS#_OSSetpts must be either equal to or less than the previous entry (RBOS1_OSSetpt2 must be less than or equal to RBOS1_OSSetpt1). This ensures the functionality of the RBOS feature in that as Acceleration increases the RBOS overspeed setpoint either stays the same or decreases, but never increases.

These restrictions are enforced by the build in ToolboxST, with errors that provide help to the user to identify the issues in their configuration.

7.1.6.3 Pulse Rate (Used on SPRO, TPRO, TREA)

Parameter	Pulse Rate Description	Choices
PRType	Selects the type of Pulse Rate Input, (For Proper Resolution)	Unused,Speed,Flow,Speed_LM,Speed_ High
PRScale	Pulses per Revolution (outputs RPM)	0 to 1,000
OSHW_Setpoint	Hardware Overspeed Trip Setpoint in RPM	0 to 20,000
OS_Setpoint	Overspeed Trip Setpoint in RPM	0 to 20,000
OS_Tst_Delta	Off Line Overspeed Test Setpoint Delta in RPM	-2,000 to 2,000
Zero_Speed	Zero Speed for this Shaft in RPM (1 RPM hysteresis), 0 RPM sets PR#_Zero always false	0 to 20,000
Min_Speed	Min Speed for this Shaft in RPM	0 to 20,000
Accel_Trip	Enable Acceleration Trip	Disable, Enable
Acc_Setpoint	Acceleration Trip Setpoint in RPM / Sec	0 to 20,000
TMR_DiffLimt	Diag Limit,TMR Input Vote Difference, in Eng Units	0 to 20,000

7.1.6.4 PT (Used on TPRO, SPRO)

Parameter	Description	Choices
PT_Input	PT primary in Eng Units (kv or percent) for PT_Output	1 to 1000
PT_Output	PT Output in Volts rms for PT_Input - typically 115	0 to 150
TMR_DiffLimt	Diag Limit,TMR Input Vote Difference, in Eng Units	1 to 1000

7.1.6.5 K25A (Used on TREG, TRES, TREL)

Parameter	K25A Description	Choices
SynchCheck	Synch Check Relay K25A Used	Used, Unused
DiagVoteEnab	Enable Voting Disagreement Diagnostic	Enable, Disable
SystemFreq	System Frequency in hz	50 Hz, 60 Hz
ReferFreq	Select Freq Refer for PLL, PR_Std input (If single shaft PR1, otherwise PR2) or from Signal Space	PR_Std or SgSpace
TurbRPM	Rated RPM, Load Turbine	0 to 20,000
VoltageDiff	Maximum Voltage Diff in Eng Units (kv or percent) for Synchronizing	1 to 1000
FreqDiff	Maximum Frequency Difference in hz for Synchronizing	0 to 0.5
PhaseDiff	Maximum Phase Difference in degrees for Synchronizing	0 to 30
GenVoltage	Allowable Minimum Gen Voltage,Eng Units (kv or percent) for Synchronizing. Typically 50% of rated	1 to 1000
BusVoltage	Allowable Minimum Bus Voltage,Eng Units (kv or percent) for Synchronizing. Typically 50% of rated	1 to 1000

7.1.6.6 Contacts (Used on TREG, TRES, TREL)

Parameter	Description	Choices
ContactInput	ContactInput	Used, Unused
SeqOfEvents	Record Contact transitions in Sequence of Events	Enable, Disable
DiagVoteEnab	Enable Voting Disagreement Diagnostic	Enable, Disable
TripMode	TripMode	Enable, Disable

7.1.6.7 E-Stop (Used on TREG)

Parameter	Description	Choices
DiagVoteEnab	Enable Voting Disagreement Diagnostic	Enable, Disable

7.1.6.8 E-Stop (Used on TREA)

Parameter	Description	Choices
EstopEnab	Enable E-Stop Detection on TREA card	Enable, Disable
DiagVoteEnab	Enable Voting Disagreement Diagnostic	Enable, Disable

7.1.6.9 Econ Relays (Used on TREG)

Parameter	Description	Choices
Signal	Relay Signal	Used, Unused
DiagVoteEnab	Enable Voting Disagreement Diagnostic	Enable, Disable

7.1.6.10 K4CL (Used on TREG, TRES, TREL)

Parameter	Description	Choices
Signal	Relay Signal	Used, Unused
DiagVoteEnab	Enable Voting Disagreement Diagnostic	Enable, Disable

7.1.6.11 ETR Relays (Used on TREA, TREG, TRES, TREL)

Parameter	Description	Choices
RelayOutput	Relay Signal	Used, Unused
DiagVoteEnab	Enable Voting Disagreement Diagnostic	Enable, Disable
DiagSolEnab	Enable Solenoid Voltage Diagnostic	Enable, Disable

7.1.6.12 Variables PPRO

Variable	PPRO Variable Description	Direction	Type	Terminal Boards
L3DIAG_PPRO_R,S,T	I/O Diagnostic Indication	Input	BOOL	All
LINK_OK_PPRO_R,S,T	I/O Link Okay Indication	Input	BOOL	
ATTN_PPRO_R,_S, and _T	I/O Attention Indication	Input	BOOL	
PS18V_PPRO_R,_S, and _T	I/O 18 V Power Supply Indication	Input	BOOL	
PS28V_PPRO_R,_S, and _T	I/O 28 V Power Supply Indication	Input	BOOL	
IOPackTmpr_R,_S, and _T	I/O Pack Temperature (deg °F)	AnalogInput	REAL	
K1FLT	K1 Shorted Contact Fault	Input	BOOL	TREA
K2FLT	K2 Shorted Contact Fault	Input	BOOL	
SilModErr	Sil Mode Configuration modification after going On Line	Input	BOOL	All
EstopModErr	E-Stop Configuration modification after going On Line	Input	BOOL	
TA_StptLoss	L30TA	Input	BOOL	
GT_1Shaft	Config – Gas Turb,1 Shaft Enabled	Input	BOOL	
GT_2Shaft	Config – Gas Turb,2 Shaft Enabled	Input	BOOL	
LM_2Shaft	Config – LM Turb,2 Shaft Enabled	Input	BOOL	
LM_3Shaft	Config – LM Turb,3 Shaft Enabled	Input	BOOL	
LargeSteam	Config – Large Steam 1, Enabled	Input	BOOL	
MediumSteam	Config – Medium Steam Enabled	Input	BOOL	
SmallSteam	Config – Small Steam Enabled	Input	BOOL	
Stag_GT_1Sh	Config – Stag 1 Shaft, Enabled	Input	BOOL	
Stag_GT_2Sh	Config – Stag 2 Shaft, Enabled	Input	BOOL	
L3SS_Comm	Communication Status - OK = True	Input	BOOL	
LokdRotorByp	LL97LR_BYP - Locked Rotor Bypass	Output	BOOL	
HPZeroSpdByp	L97ZSC_BYP - HP Zero Speed Check Bypass	Output	BOOL	

Variable	PPRO Variable Description	Direction	Type	Terminal Boards
DriveFreq	RefrFreq - Drive (Gen) Freq (Hz), used for non standard drive config	AnalogOutput	REAL	TPRO, SPRO
Speed1	Shaft Speed 1 in RPM	AnalogOutput	REAL	All
ContWdog	Controller Watchdog Counter	Output	DINT	

7.1.6.13 Variables Contacts

Variable	Contact Variable Description	Direction	Type	Terminal Boards
Contact1	Contact Input 1	Input	BOOL	TREG, TRES, TREL
Contact2	Contact Input 2	Input	BOOL	TREG, TRES, TREL
Contact3	Contact Input 3	Input	BOOL	TREG, TRES, TREL
Contact4	Contact Input 4	Input	BOOL	TREG, TRES, TREL
Contact5	Contact Input 5	Input	BOOL	TREG, TRES, TREL
Contact6	Contact Input 6	Input	BOOL	TREG, TRES, TREL
Contact7	Contact Input 7	Input	BOOL	TREG, TRES, TREL

7.1.6.14 Variables Econ Relays

Variable	Econ Relay Variable Description	Direction	Type	Terminal Boards
KE1_Fdbk	Current Economizing Relay for Trip Solenoid 1	Input	BOOL	TREG
KE2_Fdbk	Current Economizing Relay for Trip Solenoid 2	Input	BOOL	TREG
KE3_Fdbk	Current Economizing Relay for Trip Solenoid 3	Input	BOOL	TREG

7.1.6.15 Variables E-Stop

Variable	E-Stop Variable Description	Direction	Type	Terminal Boards
KESTOP1_Fdbk	ESTOP1,inverse sense,K4 relay, True = Run A SOE is generated for this variable, requiring the attachment of an application variable to this signal. Otherwise, a build warning is generated.	Input	BOOL	TREG
KESTOP1_Fdbk	ESTOP1,inverse sense,True = Run A SOE is generated for this variable, requiring the attachment of an application variable to this signal. Otherwise, a build warning is generated.	Input	BOOL	TREA

7.1.6.16 Variables ETR Relays

Variable	ETR Relay Variable Description	Direction	Type	Terminal Boards
K1_Fdbk	L4ETR1_FB, Trip Relay 1 Feedback	Input	BOOL	TREA, TREG, TRES, TREL
K2_Fdbk	L4ETR2_FB, Trip Relay 2 Feedback	Input	BOOL	TREA, TREG, TRES, TREL
K3_Fdbk	L4ETR3_FB, Trip Relay 3 Feedback	Input	BOOL	TREG, TRES, TREL

7.1.6.17 Variables Fanned-PR

Variable	Description	Direction	Type	Terminal Boards
Fan_Spd_Fbk	Fanned Speed Signal Feedback :- Fanned = Jumpers Closed	Input	BOOL	TREA

7.1.6.18 Variables K25A

Variable	Description	Direction	Type	Terminal Boards
K25A_Fdbk	Synch Check Relay When this is set to False, the generator and bus potential transformer (PT) live values are disabled.	Input	BOOL	TREG, TRES, TREL

7.1.6.19 Variables K4CL

Variable	Description	Direction	Type	Terminal Boards
K4CL_Fdbk	Drive Control Valve Servos Closed	Input	BOOL	TREG, TREL, TRES

7.1.6.20 Variables PT

Variable	Description	Direction	Type	Terminal Boards
BusPT_KVolts	Kilo-Volts RMS (Active only if K25A is Enabled)	AnalogInput	REAL	TPRO, SPRO
GenPT_KVolts	Kilo-Volts RMS (Active only if K25A is Enabled)	AnalogInput	REAL	TPRO, SPRO

7.1.6.21 Variables Pulse Rate

Variable	Description	Direction	Type	Terminal Boards
PulseRate1	HP speed	AnalogInput	REAL	TPRO, SPRO,TREA
PulseRate2	LP speed	AnalogInput	REAL	TPRO, SPRO,TREA
PulseRate3	IP speed	AnalogInput	REAL	TPRO, SPRO,TREA

7.1.6.22 Variables Vars-CI

Variable	Vars-CI Variable Description	Direction	Type	Terminal Boards
Cont1_TrEnab	Config – Contact 1 Trip Enabled – Direct	Input	BOOL	TREG, TRES, TREL
Cont2_TrEnab	Config – Contact 2 Trip Enabled – Direct	Input	BOOL	TREG, TRES, TREL
Cont3_TrEnab	Config – Contact 3 Trip Enabled – Direct	Input	BOOL	TREG, TRES, TREL
Cont4_TrEnab	Config – Contact 4 Trip Enabled – Direct	Input	BOOL	TREG, TRES, TREL
Cont5_TrEnab	Config – Contact 5 Trip Enabled – Direct	Input	BOOL	TREG, TRES, TREL
Cont6_TrEnab	Config – Contact 6 Trip Enabled – Direct	Input	BOOL	TREG, TRES, TREL
Cont7_TrEnab	Config – Contact 7 Trip Enabled – Direct	Input	BOOL	TREG, TRES, TREL
Inhbt1_Fdbk	Trip Inhibit Signal Feedback for Contact 1	Input	BOOL	TREG, TRES, TREL
Inhbt2_Fdbk	Trip Inhibit Signal Feedback for Contact 2	Input	BOOL	TREG, TRES, TREL
Inhbt3_Fdbk	Trip Inhibit Signal Feedback for Contact 3	Input	BOOL	TREG, TRES, TREL
Inhbt4_Fdbk	Trip Inhibit Signal Feedback for Contact 4	Input	BOOL	TREG, TRES, TREL
Inhbt5_Fdbk	Trip Inhibit Signal Feedback for Contact 5	Input	BOOL	TREG, TRES, TREL
Inhbt6_Fdbk	Trip Inhibit Signal Feedback for Contact 6	Input	BOOL	TREG, TRES, TREL
Inhbt7_Fdbk	Trip Inhibit Signal Feedback for Contact 7	Input	BOOL	TREG, TRES, TREL
Trip1_EnCon	Contact 1 Trip Enabled – Conditional	Input	BOOL	TREG, TRES, TREL
Trip2_EnCon	Contact 2 Trip Enabled – Conditional	Input	BOOL	TREG, TRES, TREL
Trip3_EnCon	Contact 3 Trip Enabled – Conditional	Input	BOOL	TREG, TRES, TREL
Trip4_EnCon	Contact 4 Trip Enabled – Conditional	Input	BOOL	TREG, TRES, TREL
Trip5_EnCon	Contact 5 Trip Enabled – Conditional	Input	BOOL	TREG, TRES, TREL
Trip6_EnCon	Contact 6 Trip Enabled – Conditional	Input	BOOL	TREG, TRES, TREL
Trip7_EnCon	Contact 7 Trip Enabled – Conditional	Input	BOOL	TREG, TRES, TREL
Trip1_Inhbt	Contact 1 Trip Inhibit	Output	BOOL	TREG, TRES, TREL
Trip2_Inhbt	Contact 2 Trip Inhibit	Output	BOOL	TREG, TRES, TREL
Trip3_Inhbt	Contact 3 Trip Inhibit	Output	BOOL	TREG, TRES, TREL
Trip4_Inhbt	Contact 4 Trip Inhibit	Output	BOOL	TREG, TRES, TREL
Trip5_Inhbt	Contact 5 Trip Inhibit	Output	BOOL	TREG, TRES, TREL
Trip6_Inhbt	Contact 6 Trip Inhibit	Output	BOOL	TREG, TRES, TREL
Trip7_Inhbt	Contact 7 Trip Inhibit	Output	BOOL	TREG, TRES, TREL

7.1.6.23 Variables Vars-Relay

Variable	Vars-Relay Variable Description	Direction	Type	Terminal Boards
K1_FdbkNV_R,S,T	Non Voted L4ETR1_FB, Trip Relay 1 Feedback	Input	BOOL	All
K2_FdbkNV_R,S,T	Non Voted L4ETR2_FB, Trip Relay 2 Feedback	Input	BOOL	
K3_FdbkNV_R,S,T	Non Voted L4ETR3_FB, Trip Relay 3 Feedback	Input	BOOL	TREG, TRES, TREL
SOL1_Vfdbk	When TREG,Trip Solenoid 1 Voltage	Input	BOOL	TREG
SOL2_Vfdbk	When TREG,Trip Solenoid 2 Voltage	Input	BOOL	TREG
SOL3_Vfdbk	When TREG,Trip Solenoid 3 Voltage	Input	BOOL	TREG
ETR1_Enab	Config – ETR1 Relay Enabled	Input	BOOL	All
ETR2_Enab	Config – ETR2 Relay Enabled	Input	BOOL	
ETR3_Enab	Config – ETR3 Relay Enabled	Input	BOOL	TREG, TRES, TREL
KE1_Enab	Config – Economizing Relay 1 Enabled	Input	BOOL	TREG
KE2_Enab	Config – Economizing Relay 2 Enabled	Input	BOOL	TREG
KE3_Enab	Config – Economizing Relay 3 Enabled	Input	BOOL	TREG
K4CL_Enab	Config – Servo Clamp Relay Enabled	Input	BOOL	TREG, TRES, TREL
K25A_Enab	Config – Synch Check Relay Enabled	Input	BOOL	TREG, TRES, TREL
PTR1	L20PTR1 - Primary Trip Relay CMD vs. Voltage - a Mismatch Diagnostic Monitor	Output	BOOL	All
PTR2	L20PTR2 - Primary Trip Relay CMD vs. Voltage - a Mismatch Diagnostic Monitor	Output	BOOL	
PTR3	L20PTR3 - Primary Trip Relay CMD vs. Voltage - a Mismatch Diagnostic Monitor	Output	BOOL	TREG, TRES, TREL
TestETR1	L97ETR1 - ETR1 test, True deenergizes relay	Output	BOOL	All
TestETR2	L97ETR2 - ETR2 test, True deenergizes relay	Output	BOOL	
TestETR3	L97ETR3 - ETR3 test, True deenergizes relay	Output	BOOL	TREG, TRES, TREL

7.1.6.24 Variables Vars-Speed

Variable	Vars-Speed Variable Description	Direction	Type	Terminal Boards
Acc1_TrEnab	Config – Accel 1 Trip Enabled	Input	BOOL	All
Acc2_TrEnab	Config – Accel 2 Trip Enabled	Input	BOOL	
Acc3_TrEnab	Config – Accel 3 Trip Enabled	Input	BOOL	
OS1HW_SP_Pend	Hardware HP overspeed setpoint changed after power up	Input	BOOL	
OS2HW_SP_Pend	Hardware LP overspeed setpoint changed after power up	Input	BOOL	
OS3HW_SP_Pend	Hardware IP overspeed setpoint changed after power up	Input	BOOL	
OS1HW_SP_CfgErr	Hardware HP Overspd Setpoint Config Mismatch Error	Input	BOOL	
OS2HW_SP_CfgErr	Hardware LP Overspd Setpoint Config Mismatch Error	Input	BOOL	
OS3HW_SP_CfgErr	Hardware IP Overspd Setpoint Config Mismatch Error	Input	BOOL	
OS1_SP_CfgEr	HP Overspd Setpoint Config Mismatch Error	Input	BOOL	
OS2_SP_CfgEr	LP Overspd Setpoint Config Mismatch Error	Input	BOOL	
OS3_SP_CfgEr	IP Overspd Setpoint Config Mismatch Error	Input	BOOL	
PR1_Accel	HP Accel in RPM/SEC	AnalogInput	REAL	
PR2_Accel	LP Accel in RPM/SEC	AnalogInput	REAL	
PR3_Accel	IP Accel in RPM/SEC	AnalogInput	REAL	
PR1_Max	HP Max Speed since last Zero Speed in RPM	AnalogInput	REAL	
PR2_Max	LP Max Speed since last Zero Speed in RPM	AnalogInput	REAL	
PR3_Max	IP Max Speed since last Zero Speed in RPM	AnalogInput	REAL	
OS1_Setpoint_Fbk	Current firmware overspeed setpoint for HP shaft in RPM	AnalogInput	REAL	
OS2_Setpoint_Fbk	Current firmware overspeed setpoint for LP shaft in RPM	AnalogInput	REAL	
OS3_Setpoint_Fbk	Current firmware overspeed setpoint for IP shaft in RPM	AnalogInput	REAL	
OnLineOS1Tst	L97HP_TST1 - On Line HP Overspeed Test	Output	BOOL	
OnLineOS2Tst	L97LP_TST1 - On Line LP Overspeed Test	Output	BOOL	
OnLineOS3Tst	L97IP_TST1 - On Line IP Overspeed Test	Output	BOOL	
OffLineOS1Tst	L97HP_TST2 - Off Line HP Overspeed Test	Output	BOOL	
OffLineOS2Tst	L97LP_TST2 - Off Line LP Overspeed Test	Output	BOOL	
OffLineOS3Tst	L97IP_TST2 - Off Line IP Overspeed Test	Output	BOOL	

Variable	Vars-Speed Variable Description	Direction	Type	Terminal Boards
TrpAntcptTst	L97A_TST - Trip Anticipate Test	Output	BOOL	TREG, TRES, TREL
PR_Max_Rst	Max Speed Reset	Output	BOOL	All
OnLineOS1X	L43EOST_ONL - Online HP Overspeed Test,with auto reset	Output	BOOL	
RBOS1_TestEnable	Enable Test Mode for RBOS feature for HP. RBOS1_Accel_ Test will be used as Accel input to RBOS.	Output	BOOL	
RBOS2_TestEnable	Enable Test Mode for RBOS feature for LP. RBOS2_Accel_ Test will be used as Accel input to RBOS.	Output	BOOL	
RBOS3_TestEnable	Enable Test Mode for RBOS feature for IP. RBOS3_Accel_Test will be used as Accel input to RBOS.	Output	BOOL	
OS1_Setpoint	HP Overspeed Setpoint in RPM	AnalogOutput	REAL	
OS2_Setpoint	LP Overspeed Setpoint in RPM	AnalogOutput	REAL	
OS3_Setpoint	IP Overspeed Setpoint in RPM	AnalogOutput	REAL	
OS1_TATrpSp	PR1 Overspeed Trip Setpoint in RPM for Trip Anticipate Fn	AnalogOutput	REAL	
OSHW_Setpoint1	HP Overspeed Setpoint in RPM	AnalogOutput	REAL	
OSHW_Setpoint2	LP Overspeed Setpoint in RPM	AnalogOutput	REAL	
OSHW_Setpoint3	IP Overspeed Setpoint in RPM	AnalogOutput	REAL	
RBOS1_Accel_Test	Test Accel signal for RBOS feature for HP shaft, RPM/s	AnalogOutput	REAL	
RBOS2_Accel_Test	Test Accel signal for RBOS feature for LP shaft, RPM/s	AnalogOutput	REAL	
RBOS3_Accel_Test	Test Accel signal for RBOS feature for IP shaft, RPM/s	AnalogOutput	REAL	

7.1.6.25 Variables Vars-Sync

Variable	Vars-Sync Variable Description	Direction	Type	Terminal Boards
L25A_Cmd	L25A Breaker Close Pulse	Input	BOOL	TPRO, SPRO
BusFreq	SFL2 hz	AnalogInput	REAL	TPRO, SPRO
GenFreq	DF2 hz	AnalogInput	REAL	TPRO, SPRO
GenVoltsDiff	DV_ERR KiloVolts rms - Gen Low is Negative	AnalogInput	REAL	TPRO, SPRO
GenFreqDiff	SFDIFF2 Slip hz - Gen Slow is Negative	AnalogInput	REAL	TPRO, SPRO
GenPhaseDiff	SSDIFF2 Phase degrees - Gen Lag is Negative	AnalogInput	REAL	TPRO, SPRO
SynCk_Perm	L25A_PERM - Sync Check Permissive	Output	BOOL	TPRO, SPRO
SynCk_ByPass	L25A_BYPASS - Sync Check ByPass	Output	BOOL	TPRO, SPRO

7.1.6.26 Variables Vars-Trip

Variable	Vars-Trip Variable Description	Direction	Type	Terminal Boards
ComposTrip1	Composite Trip 1	Input	BOOL	All
WatchDog_Trip	Enhanced diag - Watch Dog trip	Input	BOOL	
StaleSpeed_Trip	Enhanced diag - Stale Speed trip	Input	BOOL	
SpeedDiff_Trip	Enhanced diag - Speed Difference trip	Input	BOOL	
FrameMon_Flt	Enhanced diag - Frame Monitor Fault	Input	BOOL	
Sil_Diag_Trip	SIL Diagnostic Trip	Input	BOOL	
PR1_Zero	L14HP_ZE - HP shaft at zero speed	Input	BOOL	
PR2_Zero	L14LP_ZE - LP shaft at zero speed	Input	BOOL	
PR3_Zero	L14IP_ZE - IP shaft at zero speed	Input	BOOL	
OS1_Trip	L12HP_TP - HP overspeed trip	Input	BOOL	
OS2_Trip	L12LP_TP - LP overspeed trip	Input	BOOL	
OS3_Trip	L12IP_TP - IP overspeed trip	Input	BOOL	
Dec1_Trip	L12HP_DEC - HP de-acceleration trip *Can only be reset when pulses are able to be seen on speed input or after the I/O pack is rebooted.*	Input	BOOL	
Dec2_Trip	L12LP_DEC - LP de-acceleration trip *Can only be reset when pulses are able to be seen on speed input or after the I/O pack is rebooted.*	Input	BOOL	
Dec3_Trip	L12IP_DEC - IP de-acceleration trip *Can only be reset when pulses are able to be seen on speed input or after the I/O pack is rebooted.*	Input	BOOL	
Acc1_Trip	L12HP_ACC - HP acceleration trip	Input	BOOL	
Acc2_Trip	L12LP_ACC - LP acceleration trip	Input	BOOL	
Acc3_Trip	L12IP_ACC - IP acceleration trip	Input	BOOL	
TA_Trip	Trip Anticipate Trip,L12TA_TP	Input	BOOL	TREG, TRES, TREL

Variable	Vars-Trip Variable Description	Direction	Type	Terminal Boards
OS1HW_Trip	L12HP_HTP - HP Hardware detected overspeed trip	Input	BOOL	All
OS2HW_Trip	L12LP_HTP - LP Hardware detected overspeed trip	Input	BOOL	
OS3HW_Trip	L12IP_HTP - IP Hardware detected overspeed trip	Input	BOOL	
L5CFG1_Trip	HP Config Trip	Input	BOOL	
L5CFG2_Trip	LP Config Trip	Input	BOOL	
L5CFG3_Trip	IP Config Trip	Input	BOOL	
L5ESTOP1	ESTOP1 Trip	Input	BOOL	TREG, TREA
L5Cont1_Trip	Contact 1 Trip	Input	BOOL	TREG, TRES, TREL
L5Cont2_Trip	Contact 2 Trip	Input	BOOL	TREG, TRES, TREL
L5Cont3_Trip	Contact 3 Trip	Input	BOOL	TREG, TRES, TREL
L5Cont4_Trip	Contact 4 Trip	Input	BOOL	TREG, TRES, TREL
L5Cont5_Trip	Contact 5 Trip	Input	BOOL	TREG, TRES, TREL
L5Cont6_Trip	Contact 6 Trip	Input	BOOL	TREG, TRES, TREL
L5Cont7_Trip	Contact 7 Trip	Input	BOOL	TREG, TRES, TREL
LPShaftLock	LP Shaft Locked	Input	BOOL	All
Cross_Trip	L4Z_XTRP - Control Cross Trip	Output	BOOL	

7.1.6.27 Variables VSen

Variable	VSen Variable Description	Direction	Type	Terminal Boards
VSen1	Voltage Sensor 1 Feedback	Input	BOOL	TREA
VSen2	Voltage Sensor 2 Feedback	Input	BOOL	TREA
VSen3	Voltage Sensor 3 - Power Monitor Feedback	Input	BOOL	TREA

7.2 PPRO Specific Alarms

The following alarms are specific to the PPRO I/O pack.

40

Description Contact Excitation Voltage Test Failure

Possible Cause Voltage for the contact inputs on the trip board is not within published limits.

Solution Check source of contact excitation voltage applied to trip board.

50

Description Main Terminal Board Mismatch

Possible Cause The terminal board configured in the ToolboxST application does not match the actual hardware.

Solution Verify that the ToolboxST configuration matches the actual hardware. Build and download the configuration to the I/O pack.

51

Description Trip Board Mismatch

Possible Cause The trip board configured in the ToolboxST application does not match the actual trip board hardware.

Solution Verify that the ToolboxST configuration matches the actual hardware. Build and download the configuration to the I/O pack.

69-71

Description Trip Relay (ETR) Driver [ ] does not match commanded state

Possible Cause The driver output of the I/O pack for Emergency Trip Relay 1 (K1), ETR2 (K2), or ETR3 (K3) does not match the commanded state. This indicates that the I/O pack does not see the relay command going out the DC-62 connector into the expected terminating impedance on the trip board.

Solution

- Check the I/O pack connector seating on the terminal board.
- Check the trip board cable seating (if not TREA) and the cable integrity.
- Replace the cable, the trip board, the main terminal board, and the I/O pack.

72-74

Description Econ Relay Driver [ ] does not match commanded state

Possible Cause The driver output of the I/O pack for Economizing Relay KE1, KE2, or KE3 does not match the commanded state. This indicates that the I/O pack does not see the relay command going out the DC-62 connector into the expected terminating impedance on the trip board.

Solution

- Check the I/O pack connector seating on terminal board.
- Check the trip board cable seating and the cable integrity.
- Replace the cable, the trip board, the main terminal board, and the I/O pack.

75

Description Servo Clamp Relay Driver does not match commanded state

Possible Cause The driver output of I/O pack for K4CL does not match the commanded state. This indicates that I/O pack does not see the relay command going out the DC-62 connector into the expected terminating impedance on the trip board.

Solution

- Check the I/O pack connector seating on terminal board.
- Check the trip board cable seating and the cable integrity.
- Replace the cable, the trip board, the main terminal board, and the I/O pack.

76

Description K25A Relay (synch check) Driver does not match commanded state

Possible Cause The driver output of I/O pack for K25A does not match the commanded state. This indicates that I/O pack does not see the relay command going out the DC-62 connector into the expected terminating impedance on the trip board.

Solution

- Check the I/O pack connector seating on terminal board.
- Check the trip board cable seating and the cable integrity.
- One at a time, replace the following: the emergency trip board cable, the trip terminal board, the terminal board hosting the I/O pack, and the I/O pack.

83-85

Description Trip Relay (ETR) Contact [ ] does not match commanded state

Possible Cause

- Relay feedback from Emergency Trip Relay ETR1 (K1), ETR2 (K2), or ETR3 (K3) does not match the commanded state. This indicates that the relay feedback from the trip board does not agree with the commanded state.
- Solenoid power is not applied to the trip board.

Solution

- Check the trip board relays, as well as the cable from trip board to main terminal board (if not TREA).
- Check that solenoid power is applied to the terminal board.

86-88

Description Econ Relay Contact [ ] does not match commanded state

Possible Cause The relay feedback from Economizing Relay 1 (KE1), KE2, or KE3 does not match the commanded state. This indicates that the relay feedback from the trip board does not agree with the commanded state.

Solution Check the trip board relays, as well as the cable from trip board to main terminal board.

89

Description Servo Clamp Relay Contact does not match commanded state

Possible Cause The relay feedback from K4CL does not match the commanded state. This indicates that the relay feedback from the trip board does not agree with the commanded state.

Solution

- Check the I/O pack connector seating on the terminal board.
- Check the trip board cable seating and the cable integrity.
- Replace the cable, the trip board, the main terminal board, and the I/O pack.

90

Description K25A Relay Coil Feedback does not match commanded state

Possible Cause The relay feedback from K25A does not match the commanded state. This indicates that the relay feedback from the trip board does not agree with the commanded state. Relay feedback is taken after hardware command voting on the trip terminal board has occurred; therefore, a probable cause is that one I/O pack is not commanding the same state as the other two I/O packs.

Solution

- Verify that the K25A Relay is supported on the paired PTUR terminal board.
- Confirm that the TMR packs are commanding the same state for K25A.
- Check the I/O pack connector seating on the terminal board.
- Check the trip board cable seating and the cable integrity.
- One at a time, replace the following: the emergency trip board cable, the trip terminal board, the terminal board hosting the I/O pack, and the I/O pack.

97

Description Solenoid Power Source is missing

Possible Cause Solenoid power monitoring provided by the trip board indicates the absence of power.

Solution

- Check the source of solenoid power.
- Confirm that the wiring between the trip boards is correct.

99-101

Description Solenoid Voltage [ ] does not match commanded state

Possible Cause

- The solenoid voltage associated with K1-K3 does not match the commanded state.
- K1-K3 are closed, but no voltage is detected on the solenoid.
- Solenoid voltage was removed through another means while the I/O pack expects to detect its presence.
- The ETR state associated with this PPRO is being out voted by the other two PPROs.

Solution

- This may be due to removal of solenoid voltage through another means when the I/O pack expects to see it.
- Review the system-level trip circuit wiring and confirm the voltage should be present if the I/O pack energizes the associated trip relay.
- From the ToolboxST application, verify that the variables (typically L20PTR#) which drive the Primary Trip Relays (PTRs) in the PTUR are correctly assigned to the PPRO **Variables** tab (PTR1, PTR2, and PTR3).
- Check the pre-voted values for *ComposTrip1* under the **Vars-Trip** tab to verify that all three PPROs have the same status. If the current PPRO differs from the others, check the pre-vote status of other variables under this tab to determine the exact cause of the composite trip and correct the condition.

105

Description TREL/S, Solenoid Power, Bus A, Absent

Possible Cause TRES/TREL solenoid power A is absent. Solenoid power does not match the solenoid state for longer than 40 ms.

Note This diagnostic alarm can be turned off if required. From the PPRO **Parameters** tab, change the value of **DiagSolPwrA** to *Disable*.

Solution

- Check power applied to the trip board.
- Check the field wiring.
- Check the solenoid.
- Replace the terminal board.

106

Description TREL/S, Solenoid Power, Bus B, Absent

Possible Cause TRES/TREL solenoid power B is absent. The solenoid power does not match the solenoid state for longer than 40 ms.

Note This diagnostic alarm can be turned off if required. From the PPRO **Parameters** tab, change the value of **DiagSolPwrB** to *Disable*.

Solution

- Check power applied to the trip board.
- Check the field wiring.
- Check the solenoid.
- Replace the terminal board.

107

Description TREL/S, Solenoid Power, Bus C, Absent

Possible Cause TRES/TREL solenoid power C is absent. The solenoid power does not match The solenoid state for longer than 40 ms.

Note This diagnostic alarm can be turned off if required. From the PPRO **Parameters** tab, change the value of **DiagSolPwrC** to *Disable*.

Solution

- Check power applied to the trip board.
- Check the field wiring.
- Check the solenoid.
- Replace the terminal board.

108

Description Control Watchdog Protection Activated

Possible Cause An alarm indicates that the *ContWdog* variable has not changed for five consecutive frames. The alarm clears if changes are seen for 60 seconds.

Solution

- Verify that the *ContWdog* is connected to the output of a DEVICE_HB block and that the block is located in a task which is run at frame rate.
- Verify that the output signal from the block is changing at least once a frame.

109

Description Speed Difference Protection Activated

Possible Cause This alarm only occurs if the parameter **SpeedDifEnable** has been enabled. An alarm indicates that the difference between the output signal *Speed1* and the first I/O pack pulse rate speed is larger than the percentage **OS_DIFF** for more than three consecutive frames. The percentage is based off of the parameter **RatedRPM_TA**. The alarm clears if the difference is within limits for 60 seconds for more than three consecutive frames.

Solution Verify that the *Speed1* signal is set up correctly in the ToolboxST and that the source of the signal reflects the primary (PTUR/YTUR) pulse rate speed.

110

Description Stale Speed Protection Activated

Possible Cause The speed trip protection may be stale. This alarm can only occur if the parameter **StaleSpdEn** has been enabled. An alarm indicates that the variable *Speed1* has not changed for 100 consecutive frames. The alarm clears if the speed dithers for 60 seconds.

Solution Verify that the *Speed1* signal is set up correctly in the ToolboxST configuration, and that the source of the signal reflects the primary (PTUR/YTUR) pulse rate speed.

111

Description Frame Sync Monitor Protection Activated

Possible Cause This alarm indicates that the communication with the controller was lost for at least five consecutive frames after the I/O pack was online. The alarm clears if the frame synch is established for at least 60 seconds.

Solution Verify that the IONet is healthy. This indicates that the I/O pack is not synchronized with the Mark VIe start-of-frame signal.

112-114

Description Overspeed [ ] firmware setpoint configuration error

Possible Cause There is a firmware over-speed limit mismatch between IO signal space limit and the configuration. The current configuration file downloaded from the ToolboxST application has a different over-speed limit than the IO signal *OS[]_Setpoint*.

Solution Change the output signal designated in *OS[]_Setpoint* (**Vars-Speed** tab) to match the configuration value *OS[]_Setpoint* (**Pulse Rate** tab).

115-117

Description Overspeed [ ] hardware setpoint configuration error

Possible Cause There is a hardware over-speed limit mismatch between IO signal space limit and the configuration. The current configuration file downloaded from the ToolboxST application has a different over-speed limit than the IO signal *OSHW_Setpoint[ ]*.

Solution Change the output signal designated in *OSHW Setpoint [ ]* (**Vars-Speed** tab) to match the configuration value in *OSHW_Setpoint* (**Pulse Rate** tab).

118-120

Description Overspeed [ ] hardware setpoint changed after power up

Possible Cause This alarm always occurs when *PulseRate[ ]* parameter **OSHW_Setpoint** is changed and downloaded to the I/O pack after the turbine has started. It can also change if **PRScale** is changed to a decimal value and downloaded to the I/O pack after the turbine has started.

Solution Confirm that the limit or scale change is correct. Restart the I/O pack to force the hardware overspeed to re-initialize the limit.

121

Description TREA - K1 solid state relay shorted

Possible Cause The TREA provides voltage-based detection of relays that remain in the energized position in the six voting contacts used to provide K1. Zero voltage has been detected on one or more contacts of K1 when voltage should be present.

Solution Replace the TREA.

122

Description TREA - K2 solid state relay shorted

Possible Cause TREA provides voltage based detection of relays that remain in the energized position in the six voting contacts used to provide K2. Zero voltage has been deleted on one or more contacts of K2 when voltage should be present.

Solution Replace the TREA.

123

Description LED - Turbine RUN permissives lost

Possible Cause The RUN LED is lit red on the I/O pack because one of the RUN permissives for the turbine has been lost. The **LedDiags** parameter must be set to *Enable* to get this alarm.

Solution

- Verify the configuration of the **LedDiag** parameter.
- From the **Vars-Trip** tab, identify the condition that caused the trip.
- The condition leading to a trip condition must be cleared, and a master reset issued.

124

Description LED - Overspeed fault detected

Possible Cause The Overspeed LED is lit on the I/O pack because of a detected Trip condition. The **LedDiag** parameter must be set to *Enable* to get this alarm.

Solution

- Verify the configuration of the **LedDiag** parameter.
- The condition leading to a trip condition must be cleared, and a master reset issued.

125

Description LED - Estop detected

Possible Cause The Estop LED is lit on the I/O pack because of a detected Estop signal. The **LedDiag** parameter must be set to *Enable* to get this alarm.

Solution

- Verify the configuration of the **LedDiag** parameter.
- Remove the Estop condition, and issue a master reset.

126

Description LED - Synch fault detected

Possible Cause

- The Synch LED is lit on the I/O pack because of a failure to synchronize. The **LedDiag** parameter must be set to *Enable* to get this alarm.
- The K25A Relay is not enabled to support synchronization

Solution

- Verify the configuration of the **LedDiag** parameter.
- Verify that the K25A Relay is enabled.
- Issue a master reset to clear the alarm until the next failed attempt to synchronize.

127

Description Configuration changed after power up - running with old configuration

Possible Cause SIL related configuration parameters have changed after going online. The following parameters may not change after going online while **SilMode** is enabled:

- SILMode
- **PRType** cannot go from/to Unused
- Contact Input TripMode/Used/Unused
- **TurbineType**
- **EstopEnab** (TREA only)

Note **PRScale** may not change regardless of **SilMode**.

Solution

- From the **Parameters** tab, verify that **SilMode** is set correctly. Set the parameters to their original state and download them to the PPRO if they have been changed inadvertently.
- Refer to the error log to determine which parameter may have changed. From the ToolboxST application, right-click **IOPack** and select **Troubleshooting**, **Advanced Diagnostics**, and **Error log**.
- Remove power from the I/O pack to get the hardware to accept the new values if changes are required.

128

Description PPRO module is not SIL compatible - remain offline

Possible Cause One or more of the boards in the PPRO module is not SIL compatible. The PPRO will not go online in this condition.

Solution

- Verify that the I/O pack(s), trip board(s), and terminal board(s) are all S-board revision types. Replace all H-board revisions with their compatible S-board revisions. Refer to the PPRO help file, the section, Compatibility.
- If SIL is not required, change the **SilMode** parameter to *Disable.*

129

Description Tripped - Missing pulse rate signal

Note This diagnostic is generated from hardware detection that is only available on PPRO_1B I/O packs. PPROH1A I/O packs will not detect this condition the same way.

Possible Cause No speed input detected on a speed sensor due to the following reasons:

- Broken wire
- Sensor malfunction
- Signal conditioning malfunction

Note This condition will cause a trip on SIL3 systems.

Solution

- Examine the PreVote values for the PulseRate signals to determine which PulseRate is affected.
- Check the terminal connections for the failed speed sensor.
- Check the speed sensor gap.

130

Description Processor hardware error detected (Error Code) [ ]

Possible Cause Hardware error detected by the FPGA as follows:

- Error code 1: FPGA program changed during runtime, possibly one-time event
- Error code 2: clock oscillator error

Note These conditions cause a trip that can only be cleared with a power cycle.

Solution

- Restart the I/O pack.
- Download firmware of the I/O pack.
- Replace the I/O pack.

131

Description The configuration is not supported for SIL mode

Possible Cause **SilMode** is *Enable* and one of the following conditions is true:

- TREA is used
- TRES/L is selected
- QC Mode enabled
- Configured as a LargeSteam turbine

Note This condition causes a trip that can only be cleared by changing the configuration and restarting the I/O pack.

Solution

- Correct the configuration to be valid.
- Change **SilMode** to *Disable.*

132

Description Rate-based Overspeed detection not supported on this hardware

Possible Cause The Rate-based Overspeed (RBOS) detection feature is not enabled on this module because it is not supported on the PPROH1A. This is likely caused by installing a PPROH1A in place of a PPROS1B without updating the ToolboxST configuration.

Note If this diagnostic alarm is active, the RBOS protection feature is not running on the specified I/O module.

Solution

- Install the PPROS1B module.
- Disable the RBOS feature for all shafts.

224-239

Description Input Signal [ ] Voting Mismatch, Local=[ ], Voted=[ ]

Possible Cause Within the TMR I/O pack set, one of the same input signals does not match the other two of the same input signals.

Solution

- Adjust the TMR threshold limit or correct the cause of the difference.
- Verify that the R, S, and T I/O pack configurations are equal to the ToolboxST configuration.
- Check the I/O pack power and the networking.
- Check the I/O pack mounting on terminal board.
- Verify the operation of the device generating the specified signal.
- Verify the terminal board wiring and connections.
- Replace the I/O pack.

1064-1255

Description Logic Signal [ ] Voting Mismatch

Possible Cause Within the TMR I/O pack set, one of the same logic signals does not match the other two of the same logic signals.

Solution

- Verify that the R, S, and T I/O pack configurations are equal to the ToolboxST configuration.
- Check the I/O pack power and the networking.
- Check the I/O pack mounting on the terminal board.
- Verify the operation of the device generating the specified signal.
- Verify the terminal board wiring and connections.
- Replace the I/O pack.