GE PPRA Emergency Turbine Protection

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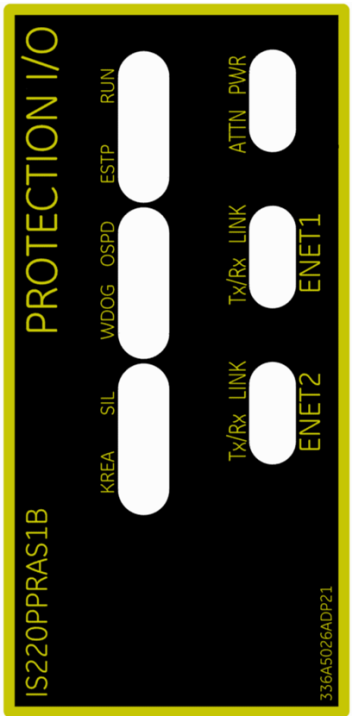
6 PPRA Emergency Turbine Protection

6.1 PPRA Emergency Turbine Protection I/O Pack



The Emergency Turbine Protection I/O packs (PPRA) and associated TREA terminal board provide an independent backup overspeed protection system. They also provide an independent watchdog function for the primary control and isolated trip contact inputs. A protection system consists of three triple modular redundant (TMR) PPRA I/O packs mounted to a TREA terminal board that has a WREA.

The PPRA supports six speed inputs fanned to three protection I/O packs in the following two configurations:

- Two speed sensors on each of three shafts
- Three speed sensors on each of two shafts.

The PPRAS1B is the only version that supports different grouping of speed inputs. The PPRA accepts six speed signals (configured as three sets of two speed inputs, or two sets of three speed inputs) for firmware overspeed, acceleration, deceleration, and a hardware implemented overspeed protection. It monitors the operation of the primary control. The PPRA monitors the status and operation of the TREA trip board through a comprehensive set of feedback signals. If a problem is detected, the PPRA will trip the backup trip relays on the TREA board and activate a trip on the primary control.

The Mark VIe control is designed with a primary and backup trip protection systems that interact at the trip terminal board level. Primary protection is provided with the Turbine Primary I/O pack (PTUR) operating a primary trip board (typically TRPA) when paired with PPRA/TREA. Backup protection is provided with PPRA mounted on a TREA terminal board. The PPRA is fully independent of and unaffected by the turbine primary protection.

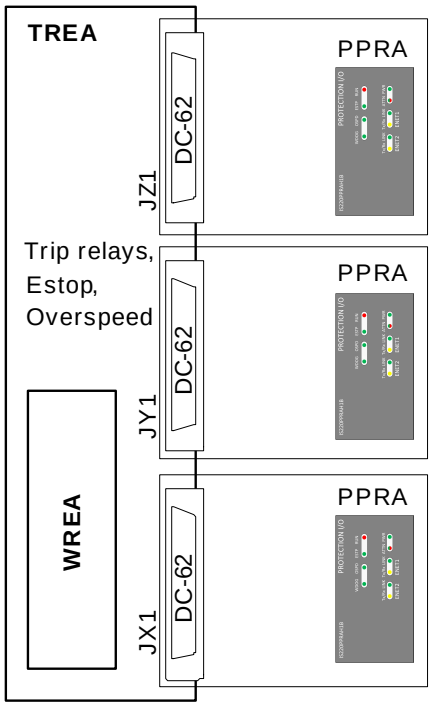
6.1.1 Compatibility

There are currently three versions of the PPRA I/O pack and each contain a functionally compatible BPPx processor board:

- The PPRAH1A contains a BPPB processor board.
- The PPRAS1A contains a BPPB processor board.
- The PPRAS1B contains a functionally compatible BPPC processor board that is supported in the ControlST***** software suite V04.07 and later. Refer to GEI-100709, Mark VIe Control PPROS1B and PPRAS1x Functional Safety Instruction Guide for proper safety loop operation and restrictions.

The PPRAS1A and S1B are IEC 61508 certified versions for use in IEC 61511 certified safety loops. The PPRAS1A or S1B with TREAS#A and WREAS1A are the safety certified versions.

The PPRA mounts directly on TREA, and with TREA it is required to have the WREA option board mounted on the PPRA application specific circuit board *Option Header* connector. The PPRA mounted on TREA with WREA will only function correctly with three PPRA I/O packs. Single and dual pack operation is not possible.



Attention

Only PPRAS1A and PPRAS1B I/O packs mounted on TREAS1A terminal boards can be configured for SIL applications.

6.1.2 Installation

➢ **To install the PPRA I/O pack**

1. Securely mount the TREA terminal board.
2. Directly plug three PPRA I/O packs into the TREA.
3. Slide the threaded posts on PPRA, located on each side of the Ethernet ports, into the slots on the terminal board mounting-bracket. Adjust the bracket location so the DC-62 pin connector on PPRA and the terminal board fit together securely. Tighten the mounting bracket. The adjustment should only be required once in the service life of the product. Securely tighten the nuts on the threaded posts locking PPRA in place.
4. Plug in one or two Ethernet cables depending on the *controller and network redundancy*. PPRA is not sensitive to Ethernet connections and selects the proper operation over either port.
5. Apply power by plugging in the power connector on the side of the module. The I/O module has inherent soft-start capability that controls current levels upon application.
6. Use the ToolboxST* application to configure the module as necessary.

6.1.2.1 Controller and Network Redundancy

In systems with a single controller, the controller R network should be connected to the PPRA on the JX1 connector, the S network should be connected to PPRA on the JY1 connector, and the T network should be connected to the PPRA on the JZ1 connector. All three networks are coming from the single controller. PPRA applications do not support dual network connections for all three PPRAs. In a redundant system there is no additional system reliability gained by adding network connections to the first two PPRAs with dual controllers or any of the three PPRAs with TMR controllers.

In systems with dual controllers, the controller R network should be connected to the PPRA on the JX1 connector, the S network should be connected to PPRA on the JY1 connector, and both the R and S networks should be connected to the PPRA on the JZ1 connector.

In systems with three controllers, the R network should be connected to the PPRA on the JX1 connector, the S network should be connected to PPRA on the JY1 connector, and the T network should be connected to the PPRA on the JZ1 connector.

6.1.3 Operation

Refer to the following sections in the *GEH-6721_Vol_II*, the chapter, *Common Module Content*:

- *Auto-reconfiguration*
- *BPPx Processor*
- *Processor LEDs*
- *Power Management*
- *ID Line*

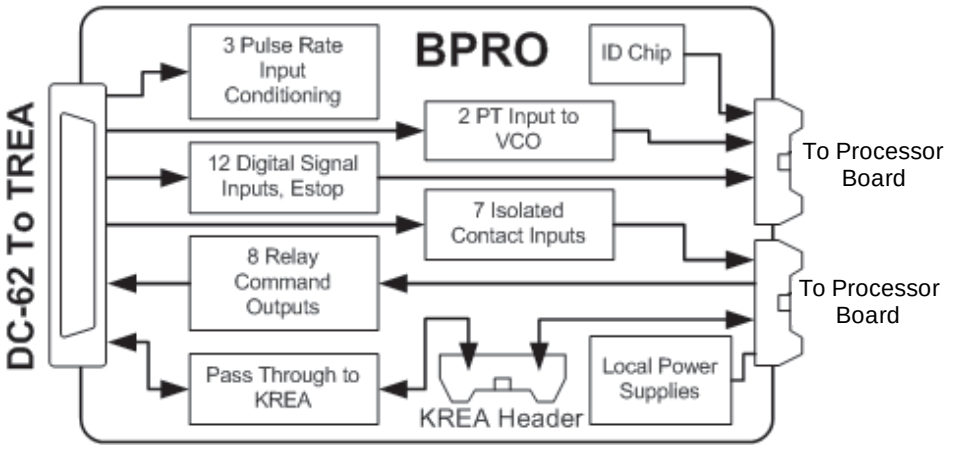
6.1.3.1 Connectors

- A DC-62 pin connector on the underside of the PPRA I/O pack connects directly to the terminal board. The connector contains the signals needed to sense inputs and operate a trip terminal board.
- An RJ-45 Ethernet connector named ENET1 on the side of the pack is the primary IONET-EGD connection.
- A second RJ-45 Ethernet connector named ENET2 on the side of the pack is the redundant or IONET-EGD connection used on dual network configurations.
- A 3-pin power connector on the side of the pack is for 28 V dc power for the pack and terminal board.

Note The TREA trip terminal board plus WREA features contact trip inputs. The power for those contacts is provided through a separate terminal board connector, not from the 28 V dc power source.

6.1.3.2 Application Hardware

The PPRA I/O pack has an internal application specific circuit board that contains the hardware needed for the emergency trip function. The application board connects between the processor and the TREA terminal board and is common between PPRA and PPRO I/O packs. The application board has an option card header that connects to a PPRA-specific option card. The following diagram displays the functions of the application board.



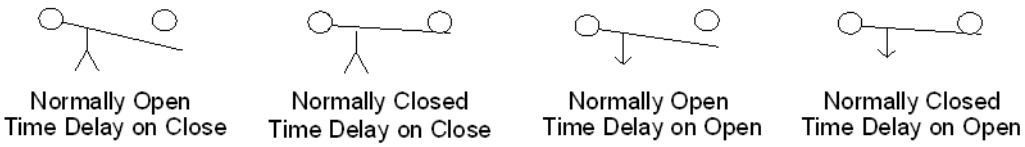
PPRA Application Specific Circuit Board

In the PPRA not all of the signal conditioning is used. The option card connected to the internal header adds support for three additional pulse rate input channels and support for the speed pulse rate repeater outputs.

All boards within the pack contain electronic ID parts that are read during power application. A similar part located with each terminal board connector allows the processor to confirm correct matching of the I/O pack to the terminal board and to report board revision status to the system level control.

6.1.3.3 Protective Functions

The PPRA performs the following protective functions in a mix of hardware, programmable logic, and firmware. In the following diagram, standard symbols for time delay contacts have been used:



In the following diagrams, a standard has been used to indicate signal origin and flow.

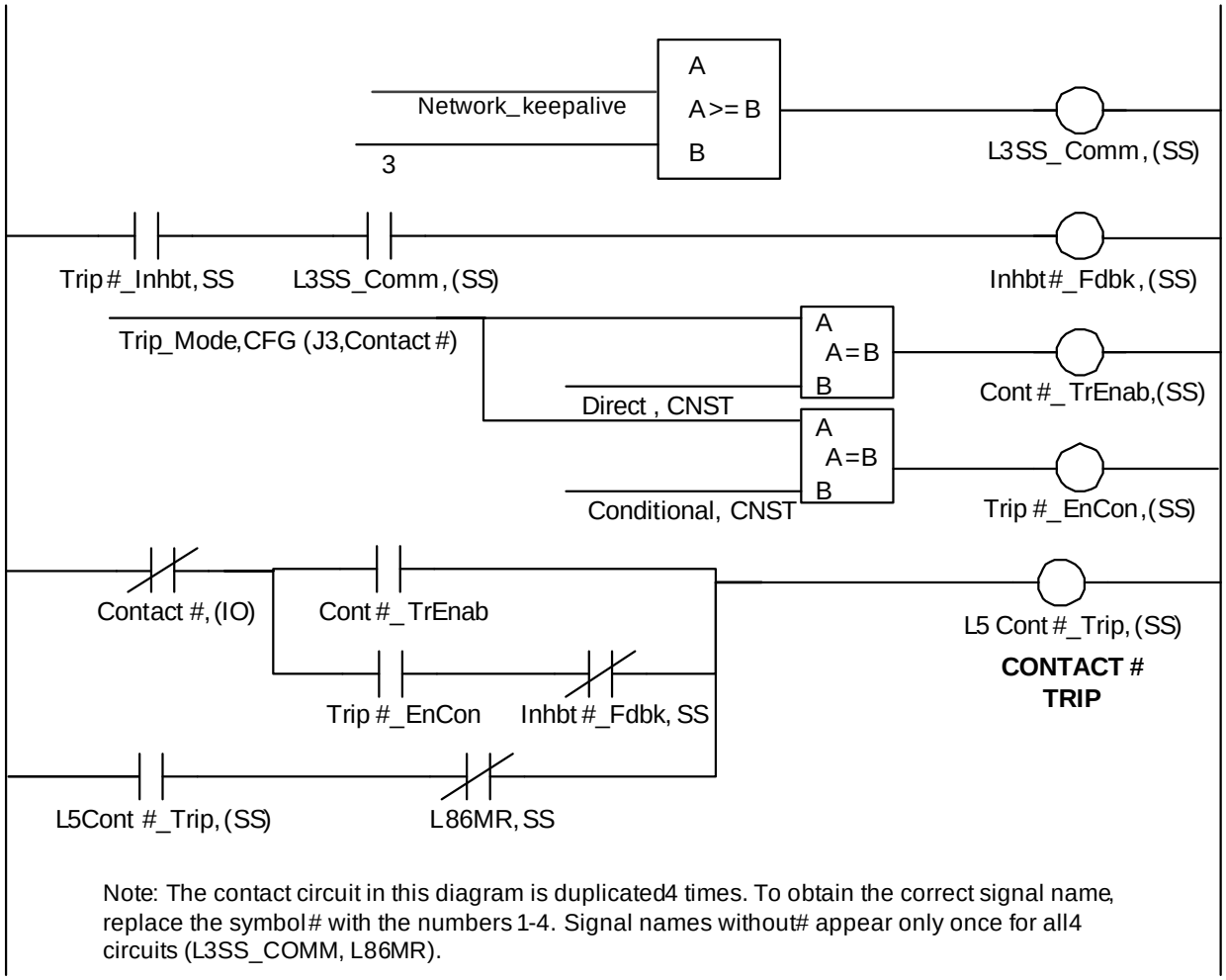
- Signal names that end with (SS) are created within PPRA and the data flow is out to the controller through signal space.
- Signal names that end with SS are created in the controller and the data flow is into PPRA through signal space.
- Signal names that end with (IO) are created within PPRA and the data flow is out to the hardware.
- Signal names that end with IO indicate the signal is a hardware input into PPRA.
- Signal names that end with anything containing CFG are part of the PPRA configuration. In this case an attempt has been made to indicate what area of the PPRA configuration contains the variable.
- When J3 is referenced in a CFG, it refers to the connection point for the trip relay board, TREA, and the corresponding configuration values.
- The combination IO (SS) indicates a signal that comes from the hardware inputs to PPRA, and is then sent out to the controller as part of signal space.

If there is no special ending on a signal name, then the signal is used internal to PPRA and is not part of the hardware or signal-space data movement. This signal is not available or visible to applications, but it is needed to adequately describe the I/O pack's operation.

6.1.3.4 Direct/Conditional Discrete Input Trip

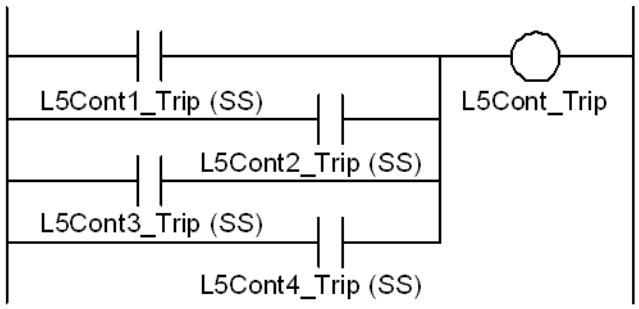
PPRA supports the four isolated discrete contact input trip signals provided on the TREA+WREA board. In the following figure, the direct / conditional determination is implemented in firmware while Contact # and L5Cont #_Trip are in hardware logic. When configured for direct trip, the firmware is not in the trip path. When configured for conditional trip, the firmware determines the communication health (displayed as network_keepalive) and populates the programmable logic with the conditional signal from signal space. If the controller communication is lost, the default will permit any conditional trip.

Note The contact inputs include an 8 ms contact de-bounce filter to protect against false trips.



PPRA Contact Input Trips

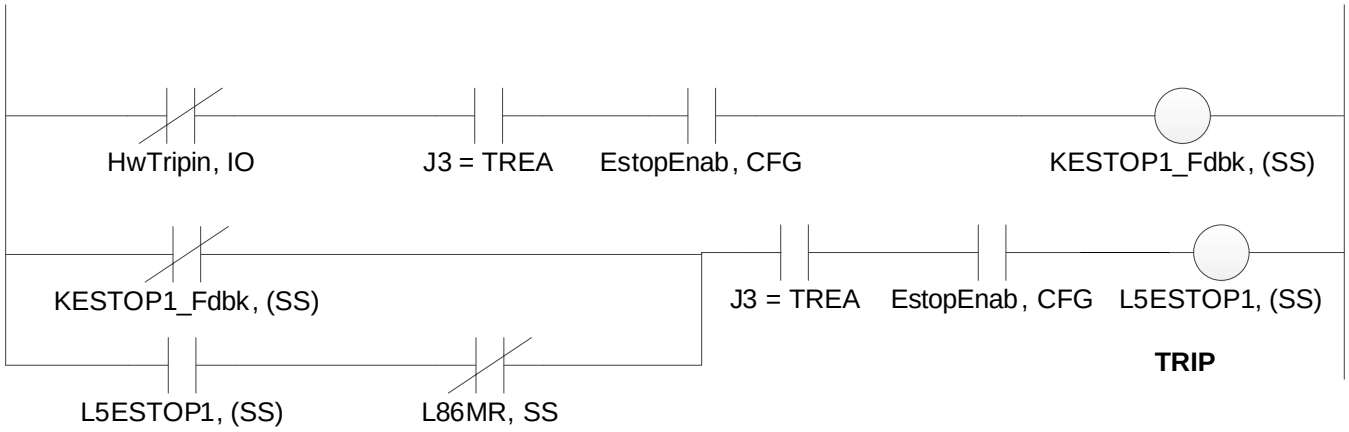
The resulting contact trip signals are combined into a single contact trip summary, L5Cont_Trip.



Contact Input Trip Signal Concentration

6.1.3.5 Trip Input

PPRA monitors a trip input signal that is present on the TREA board and uses it to cross trip the main control in the event the trip input is activated. It is also used within the pack logic as part of the trip relay output command. The relays are not required to close if the trip input signal is present. The main control counterpart is also present. If the main control votes to trip, it can also cross-trip the corresponding PPRA.



Contact Input Trip Input

Note There are several inversions in the hardware signal path, but the end result is that KESTOP#_Fdbk is only a 1 when E-Stop is energized. Therefore, 1 = OK.

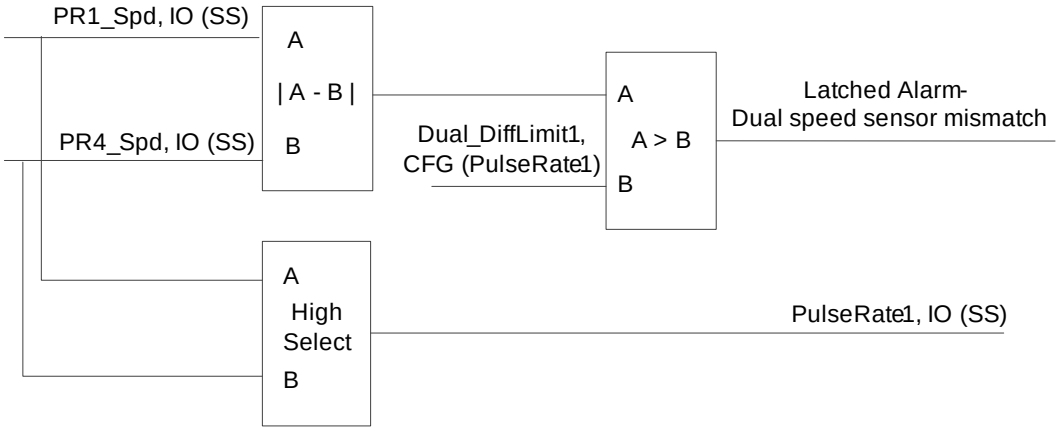
6.1.3.6 PPRA Speed Input High Select

When PRGrouping is set to ThreeGroups, PPRA speed inputs are expected to be in pairs on each shaft with up to three shafts possible (other combinations of speed inputs are not permitted). The following table displays the TREA input screw pairs for the primary (PulseRate_A) and secondary (PulseRate_B) speed signals, signal space (SS).

TREA Input Screw Pair (TB#)	Speed Variable	High-selected value
PR1H_X (43) – PR1L_X (44)	PR1_Spd (SS)	PulseRate1 (SS) (Shaft 1)
PR4H (25) – PR4L (26)	PR4_Spd (SS)	
PR2H_X (45) – PR2L_X (46)	PR2_Spd (SS)	PulseRate2 (SS) (Shaft 2)
PR5H (27) – PR5L (28)	PR5_Spd (SS)	
PR3H_X (47) – PR3L_X (48)	PR3_Spd (SS)	PulseRate3 (SS) (Shaft 3)
PR6H (29) – PR6L (30)	PR6_Spd (SS)	

Configuration of the speed inputs is done at the PulseRate1-3 level. PPRA then applies the PulseRate1 configuration values to both PR1_Spd and PR4_Spd. This ensures that the two inputs that go through a high select are configured the same.

Paired speed inputs should be the same value during normal operation. Protection for excessive difference between the two inputs is provided. The difference is calculated and compared to a configurable threshold, *Dual_DiffLimit* (default 25 rpm). If the difference exceeds the threshold a diagnostic alarm is created, *Dual speed sensors mismatch*.



Shaft Speed High Select, Difference Alarm

The high select diagram displays the overspeed names used for the first of three pulse rate inputs. The same figure is repeated for PulseRate2 and 3. For all variables where the number 1 displays, simply substitute a 2 or 3 for the 1 to get the signal name.

Note Speed inputs are sensitive to the mV level. To avoid speed difference diagnostics, unused speed input screw pairs should be electrically tied together.

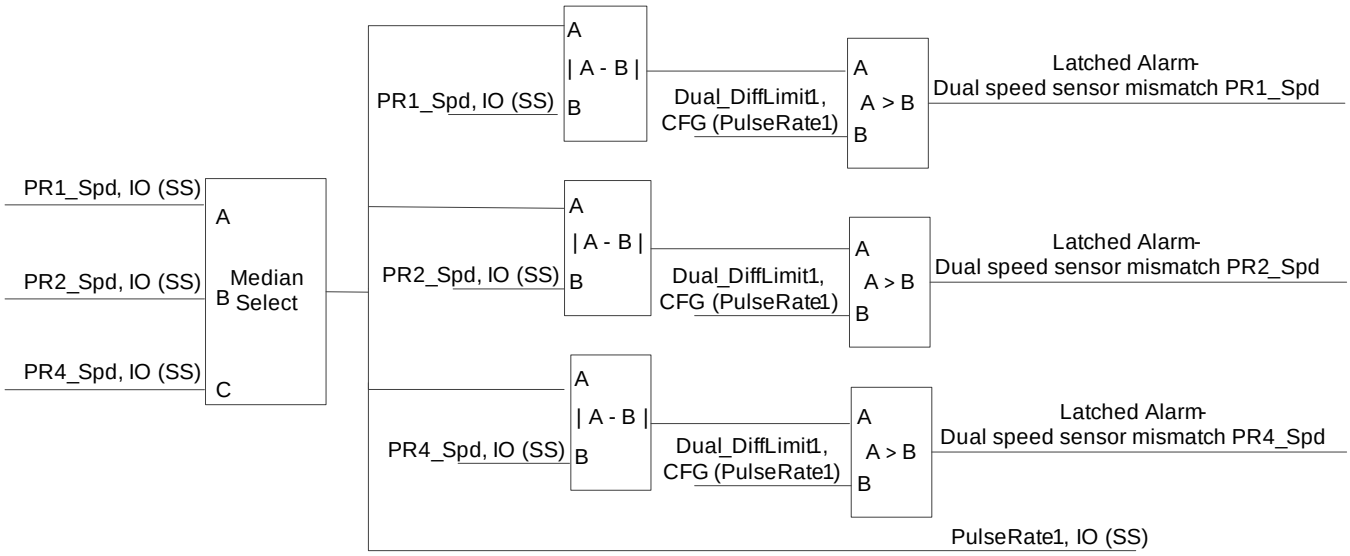
6.1.3.7 PPRA Speed Input Median Select

When **PRGrouping** is set to *TwoGroups*, PPRA speed inputs are expected to be in groups of three with up to two shafts possible (other combinations of speed inputs are not permitted). The following table displays the TREA input screw sets for the speed signals, signal space (SS).

TREA Input Screw Pair (TB#)	Speed Variable	Mid-Select value
PR1H_X(43) - PR1L_X(44)	PR1_Spd (SS)	PulseRate1(SS) (Shaft 1)
PR2H_X(45) - PR2L_X(46)	PR2_Spd (SS)	
PR4H(25) - PR4L(26)	PR4_Spd (SS)	
PR3H_X(47) - PR3L_X(48)	PR3_Spd (SS)	PulseRate2(SS) (Shaft 2)
PR5H(27) - PR5L(28)	PR5_Spd (SS)	
PR6H(29) - PR6L(30)	PR6_Spd (SS)	
N/A	N/A	PulseRate3(SS)

Configuration of the speed inputs is done at the PulseRate1-2 level. PPRA then applies the PulseRate1 configuration values to *PR1_Spd*, *PR2_Spd*, *and PR4_Spd*. This ensures that the three inputs that go through the median select are configured the same.

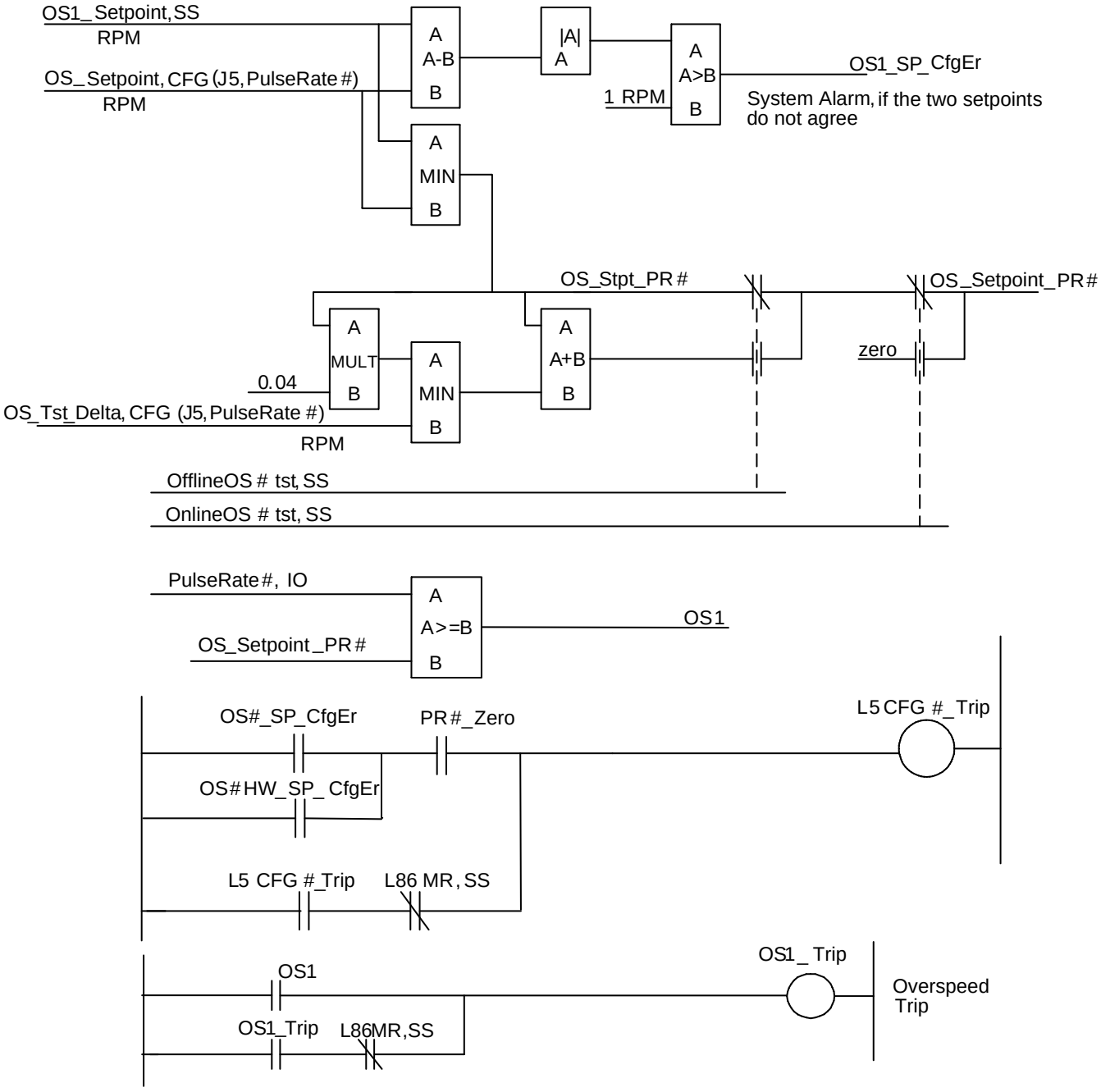
Grouped speed inputs should be the same value during normal operation. Protection for excessive difference between any two inputs in a group is provided. The difference is calculated and compared to a configurable threshold, *Dual_DiffLimit* (default 25 rpm). If the difference of any one speed in a group from the voted median value exceeds the threshold, a diagnostic alarm is generated (Dual speed sensors mismatch).



Shaft Speed Median Select, Difference Alarm

6.1.3.8 Firmware Overspeed Trip

Firmware overspeed protection is performed on the three values that come out of the high speed select. Although the established standard for naming these three inputs is HP, IP, and LP, the three inputs are free to be applied as needed in a system design. The following pulse rate variables are displayed using a # symbol. Replace the # with 1 for HP, 2 for LP, or 3 for IP.



Firmware Overspeed Trip

Firmware Overspeed Trip functions include:

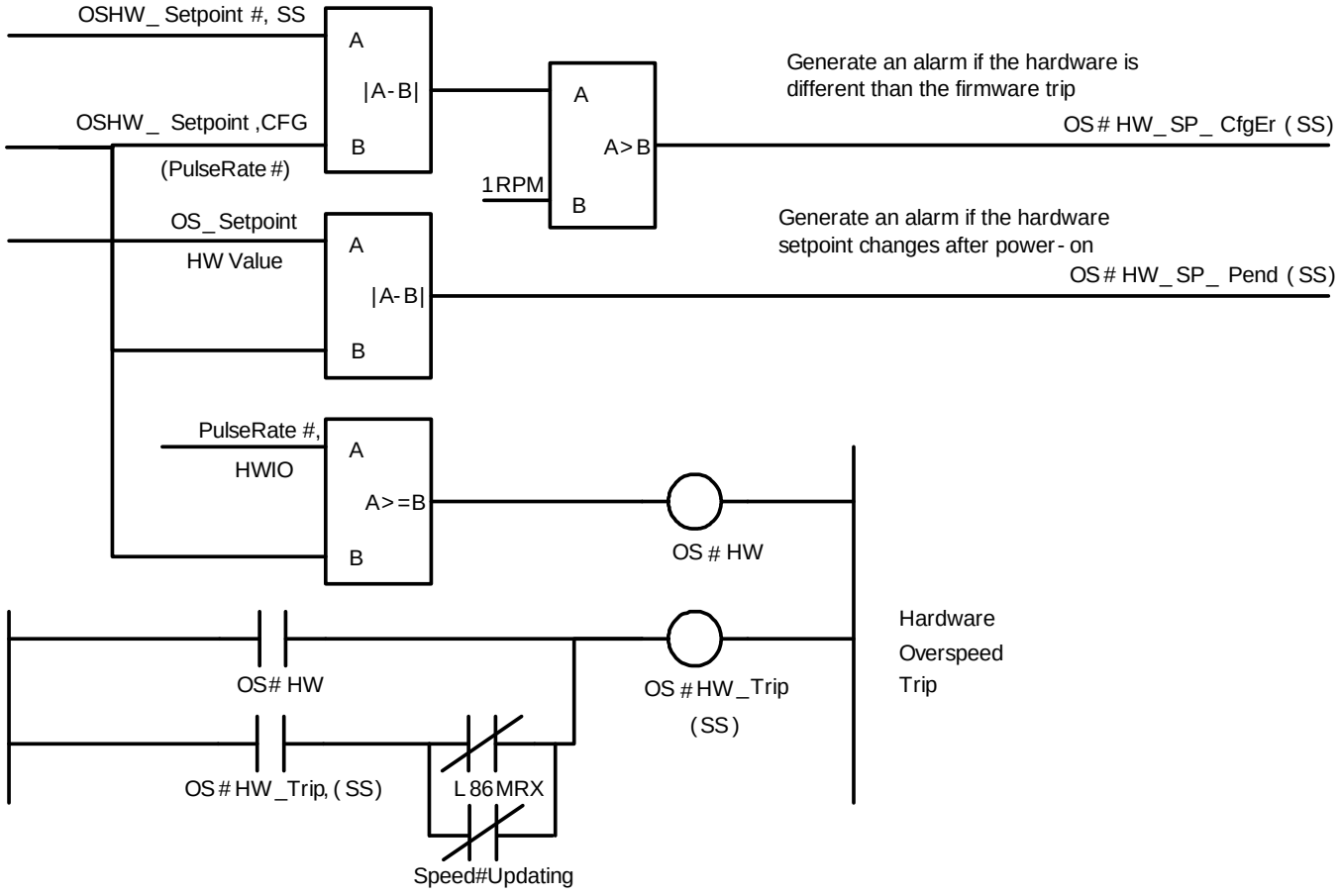
- Fault on overspeed threshold match failure between config and signal space values when speed is zero
- Pick the lower threshold from config or signal space
- Provide a mechanism to zero the threshold for online overspeed test
- Provide a mechanism to modify the threshold for offline overspeed test, bounded to limit increases to the threshold to 104%

Note Use a negative OS_Tst_Delta value to reduce the threshold during testing.

- Compare the threshold to the calculated speed and latch overspeed

6.1.3.9 PPRA Hardware Overspeed Trip

The following figure displays the overspeed names used for the first of three pulse rate input groupings. The configuration, alarms, and latched trip are performed for the pair of inputs: PR1_Spd and PR4_Spd. A detected overspeed on either PR1_ Spd or PR4_Spd will latch as OS1HW_Trip. The same groupings are repeated for pairs PR2_Spd, PR5_Spd, and PR3_Spd, PR6_Spd. The pulse rate variables are displayed using a # symbol. Replace the # with 1 for HP, 2 for LP, or 3 for IP.



Hardware Overspeed Trip, HP Shaft

Note Refer to the section, ***Shaft Speed Accel, Decel, and Zero*** for the definition of Speed#Updating

Hardware Overspeed Trip functions include:

- Load the independent hardware overspeed set point only when the PPRA pack re-boots or has power cycled
- Generate an alarm when the hardware config set point is >1 Hz different from the value passed through signal space from the application configuration
- Generate an alarm and signal space Boolean logic change when the setpoint in config fails to match the value stored in the hardware
- Implement speed calculation and the trip logic entirely inside programmable logic
- Overspeed response time will be < 20 ms at trip speed
- Hardware overspeed response in less than three rotations of the shaft (typically less than 60 ms at normal operating speeds)
- Hardware overspeed is implemented for each of the six speed inputs. The configuration and trip indication is done using the same groupings identified for firmware overspeed

For a PRGrouping of TwoGroups, the configuration, alarms, and latched trip are performed for the group of inputs: PR1_Spd, PR2_Spd, and PR4_Spd. A detected overspeed on either PR1_Spd, PR2_Spd, or PR4_Spd will latch as OS1HW_Trip. The same figure is repeated for the second grouping of PR3_Spd, PR5_Spd, and PR6_Spd. In the signal name for all variables, the number 1 can replaced by a 2, as applicable.

Note There is no separate enable or disable signal for this Overspeed protection. The disable signal is created by setting a high overspeed point value. The calculated speed will never reach the value needed to trigger OS1HW.

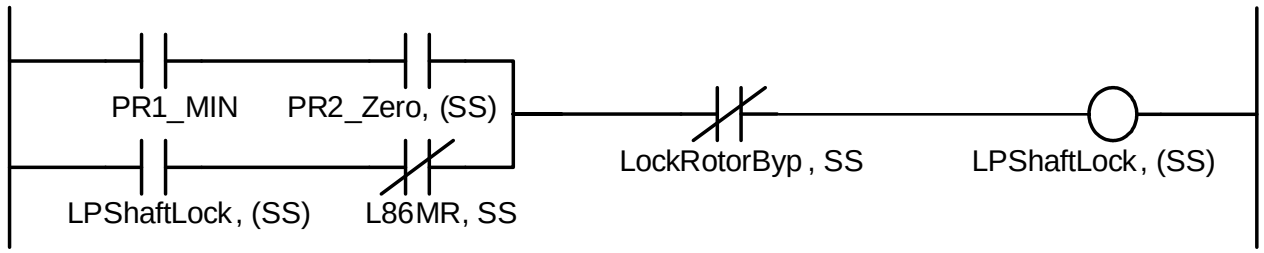
The actual hardware implementation depends on two configuration items:

- OSHW_Setpoint specifies the overspeed trip level in RPM
- PRScale determines the number of speed sensor pulses per revolution used to convert pulse rate into RPM for both hardware and firmware overspeed value

The hardware implementation requires two adjacent revolutions exceeding the OSHW _Setpoint to trip the system. When a trip is present, the setting of OSHW _Setpoint is reduced by a small amount in the hardware to provide a clean trip signal. Because there are set limits to the time integration used in the hardware detector, the minimum RPM setting for the OSHW _Setpoint is approximately four RPM.

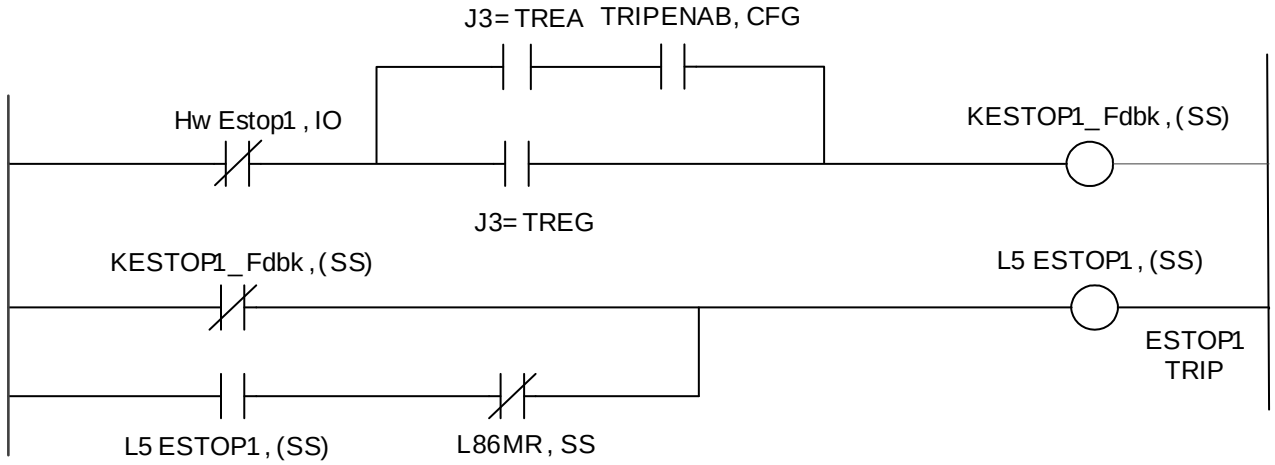
6.1.3.10 LP Shaft Locked Detection

There is another protection function in addition to the overspeed protection displayed on the preceding page. It generates a signal in the event the first pulse rate signal is above minimum speed, and the second pulse rate signal is still at zero.



6.1.3.11 E-Stop

The I/O pack monitors the E-Stop trip signal that is present on the TREG or TREA terminal boards and uses it to cross trip the main control in the event E-Stop is invoked. It is also used within the pack logic as part of the trip relay output command. The relays are not required to close if the E-Stop signal is present. The main control counterpart is also present. If the main control votes to trip, it can also cross-trip the corresponding I/O pack.

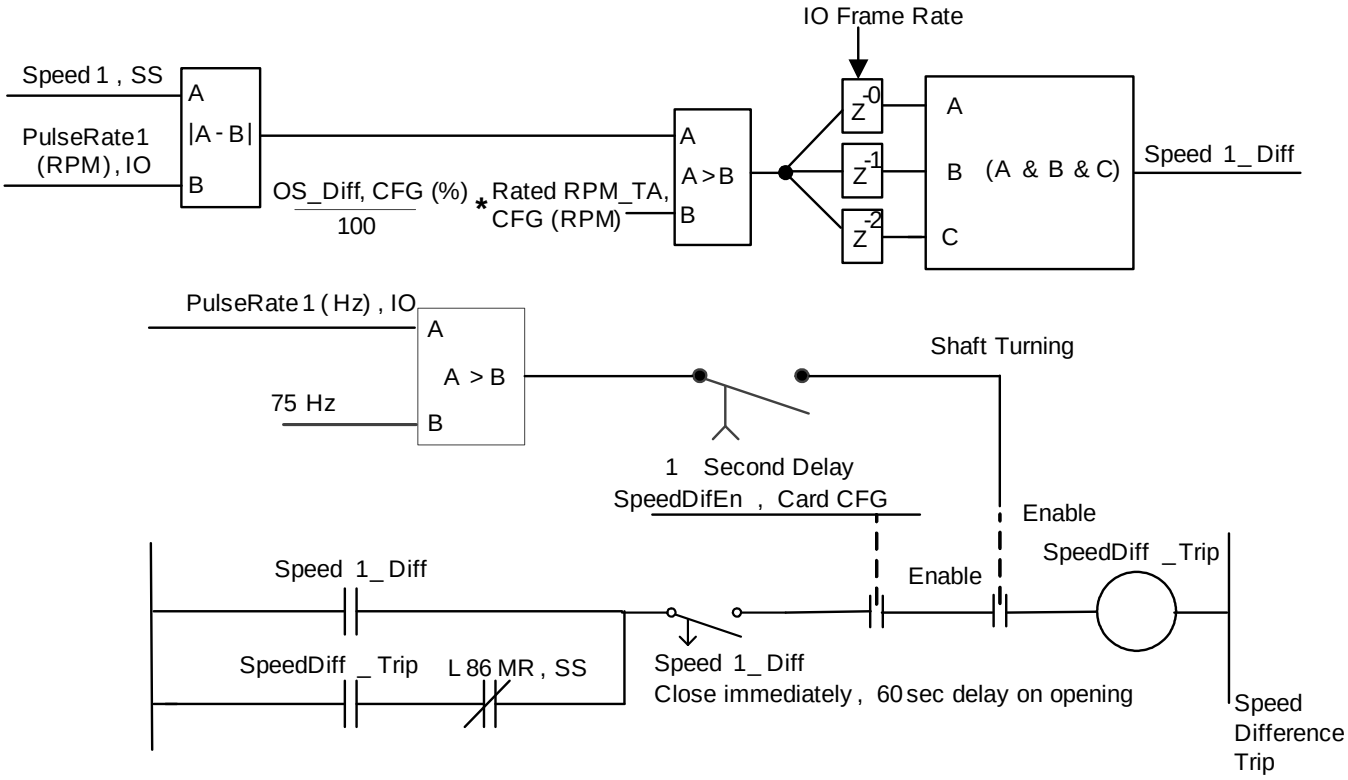


Contact Input E-Stop

Note There are several inversions in the hardware signal path, but the end result is that KESTOP#_Fdbk is only a 1 when E-Stop is energized. Therefore, 1 = OK. The TREL and TRES terminal boards do not have E-Stop capability because it is on the primary trip boards TRPL and TRPS.

6.1.3.12 Speed Difference Detection

There should never be a reason why the speed calculated by the I/O pack is significantly different from the speed calculated by the main control. Speed difference detection looks at the difference in magnitude between pulse rate 1 from both the pack and the main control. If the difference is greater than the set threshold for three successive samples, a *SpeedDifTrip* is latched. If the main control recovers for 60 seconds, the trip is removed. This allows the main control to recover with subsequent re-arming of the backup protection.



When configured for dual controller, additional logic is added so that separate speed inputs from the two controllers come into the I/O pack. This trip logic acts as if both controllers have a speed error, but continues to run if one controller has a valid speed signal.

6.1.3.13 Maximum Speed Hold

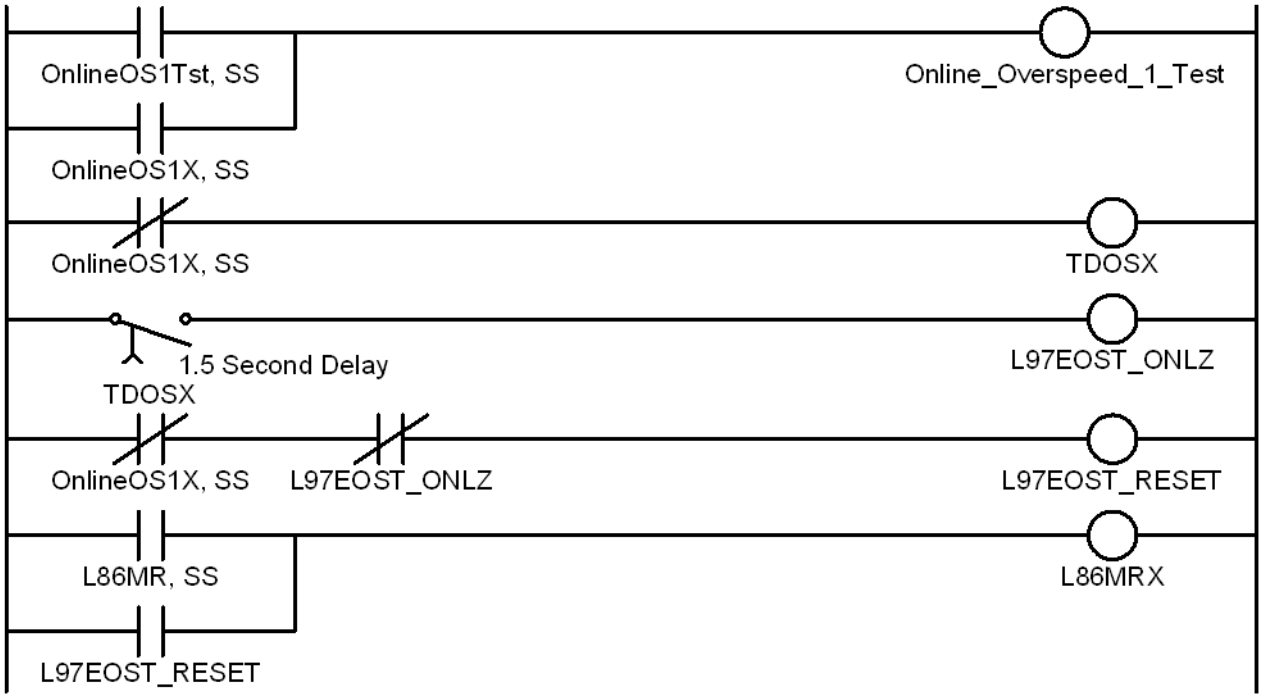
The I/O pack provides a maximum speed hold function that resets when:

- Using the command PR_Max_RST (from signal space)
- PR1_Zero changes to false when the shaft first starts turning

Output values are PR1_Max, PR2_Max, and PR3_Max. These signals are used to determine the maximum speed obtained while running or after stopping a turbine.

6.1.3.14 Overspeed Test Logic, Steam Turbine

The signal OnLineOS1Tst is used for PulseRate1, OnLineOS2Tst is used for PulseRate2, and OnLineOS3Tst is used for PulseRate3. In the following figure, there is another signal, Online OS1X, which initiates an online overspeed test for PulseRate1. This signal also creates a 1.5 second reset pulse when removed.



Online Overspeed Test Logic

6.1.3.15 Speed State Boolean Values

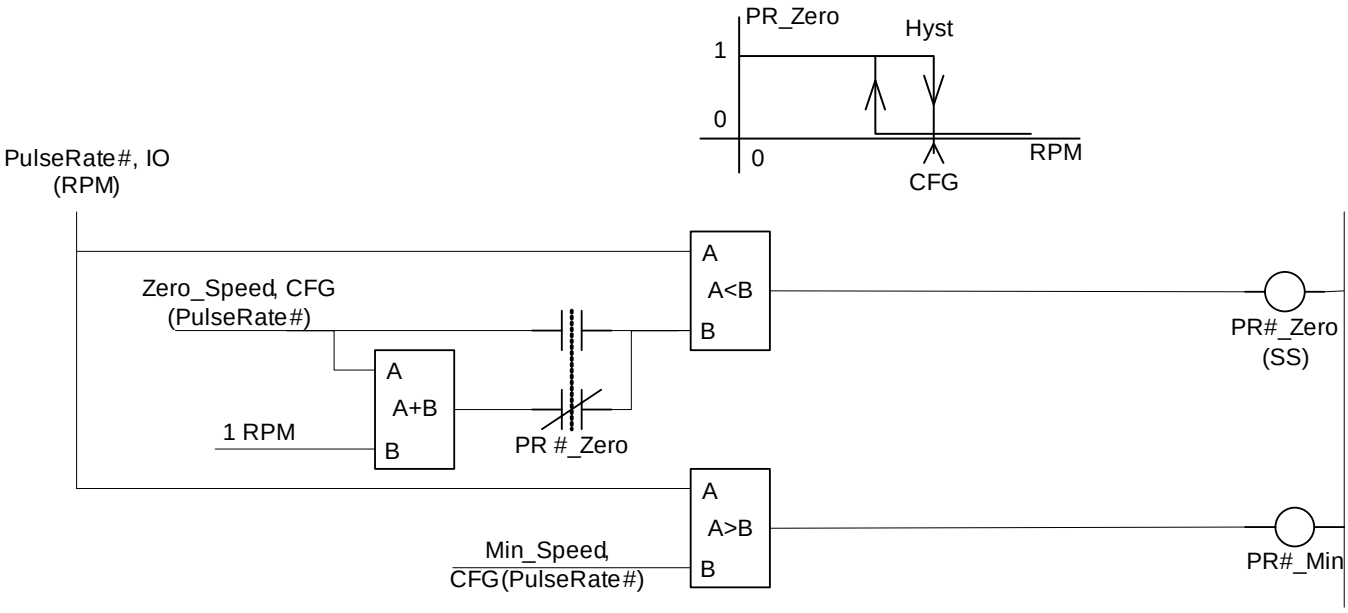
The I/O pack has detection for zero speed from a set point with 1 RPM hysteresis. The I/O pack calculates a minimum speed signal from a set point. The rate of change of speed from a set point is calculated resulting in a selectable acceleration trip. A deceleration trip is then determined from a fixed 100% / second rate.

6.1.3.16 Shaft Speed Accel, Decel and Zero

The I/O pack has detection for zero speed from a set point with 1 RPM hysteresis. The I/O pack calculates a minimum speed signal from a set point. The rate of change of speed from a set point is calculated, resulting in a selectable acceleration trip. A deceleration trip is then determined from a fixed 100% / second rate.

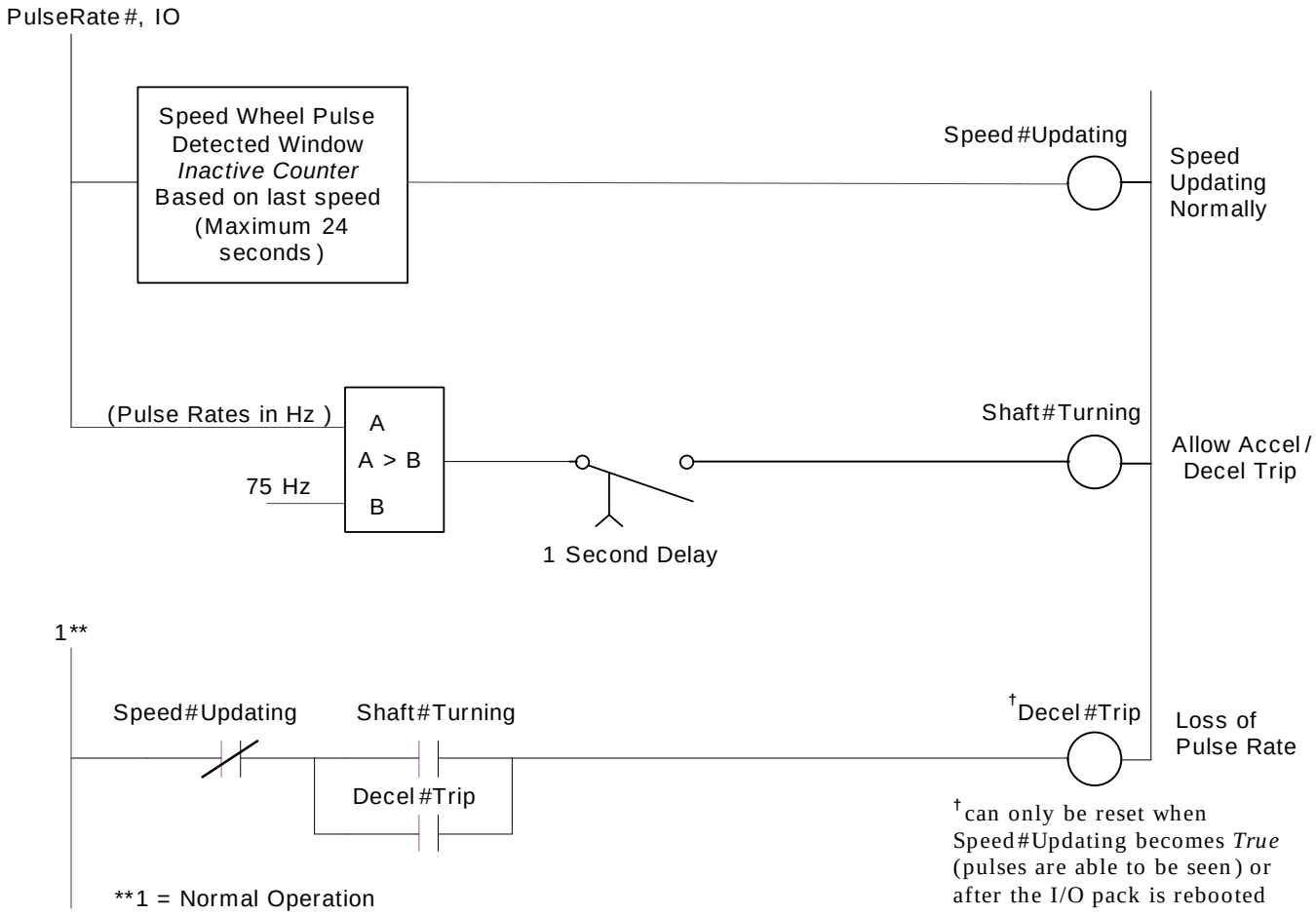
The acceleration for a given pulse rate (*PR#_Accel*) is calculated by computing two adjacent shaft speeds over a period of AccelCalType ms each by computing change in pulse counts, and then computing the difference in these speeds divided by AccelCalType ms to get the acceleration of the shaft.

In the following figures, pulse rate variables are displayed using a # symbol. Replace the # with 1 for HP, 2 for LP, or 3 for IP. This figure is the same for PulseRate1, 2, and 3. Simply replace the 1 with a 2 or 3 to get the signal name. The contact, PR#_ Min, in the Acc1_Trip is only present for PR2 (PR2_Min) and PR3 (PR3_Min). It is not used for PR1.

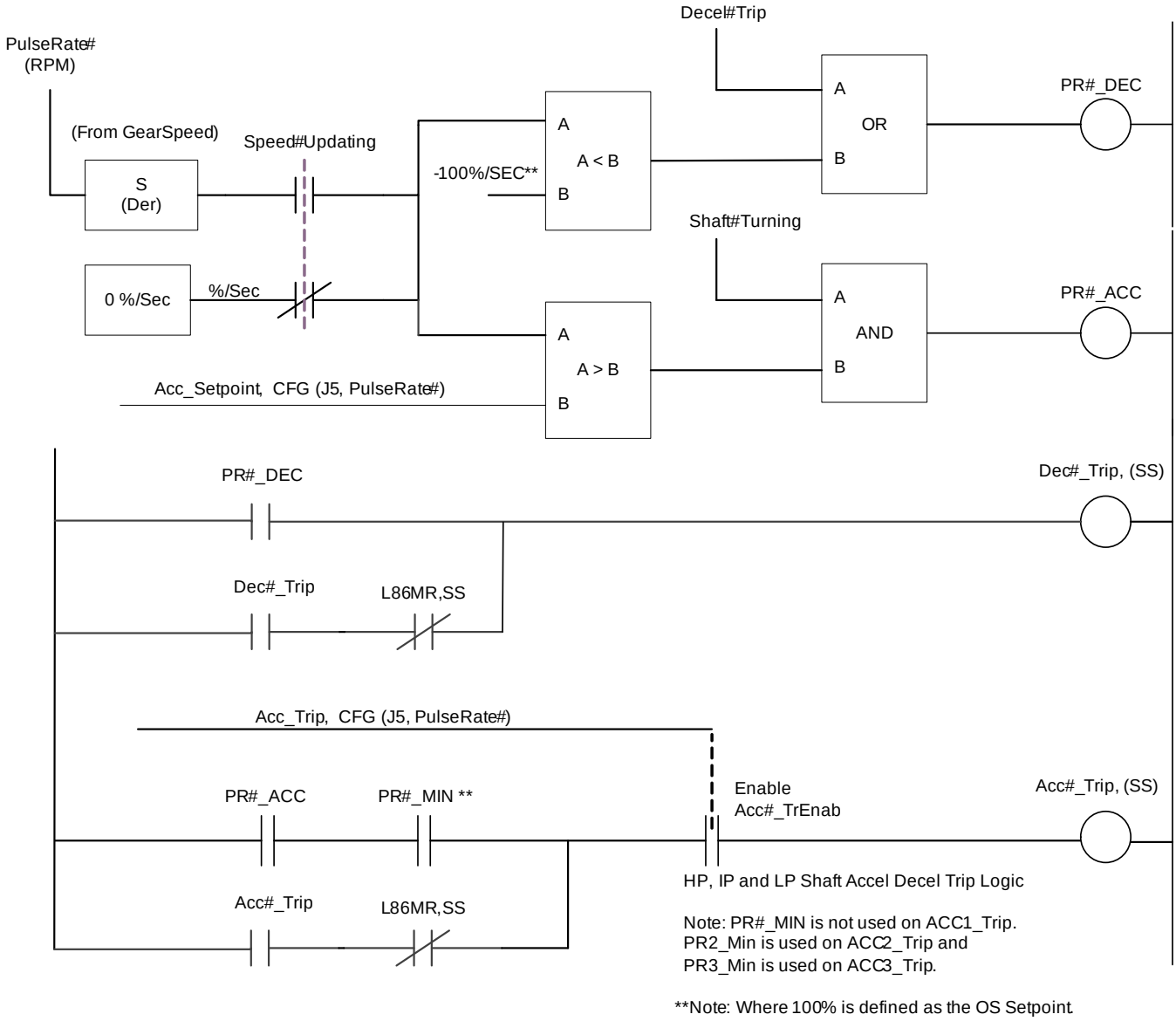


Speed State Boolean Values

The pulse rate inputs have special detection for loss of signal, and special filtering to remove input noise from nearly stationary shaft speeds.



Pulse Rate Conditioning



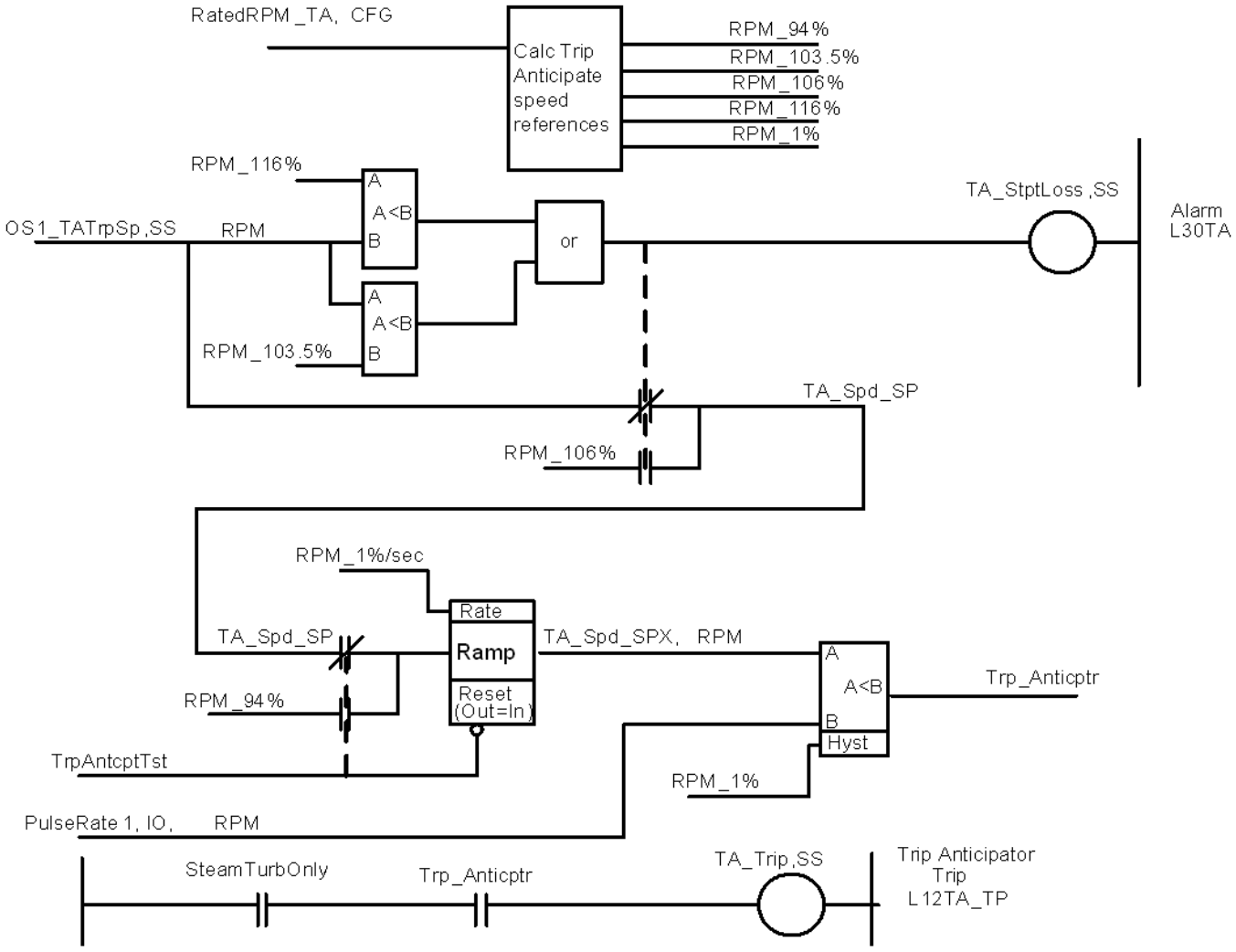
Shaft Speed Accel, Decel and Zero

6.1.3.17 Trip Anticipate Function

Steam turbine applications provide a speed trip that uses a live set point from signal space. This overspeed trip is vigorously changed as a function of turbine load. This function does the following:

- Input set point is OS1_TATrpSp from signal space. Input rated RPM is specified by RatedRPM_TA as part of the I/O pack configuration. Function test request input is TrpAntcptTst from signal space.
- If (OS1_TATrpSP is < 103.5% OR > 116% of RatedRPM_TA) then TA_Spd_Sp (the local set point value) = 106% of RatedRPM_TA and TA_StptLoss (Signal space) is true and alarm L30TA is declared. Otherwise, TA_Spd_Sp = OS1_ TATrpSP.
- If TrpAntcptTst is true, decrease the current value of TA_Spd_Sp by 1RPM / second. Set the minimum value of RatedRPM_TA to 94%. If TrpAntcptTst is false, the value of TA_Spd_Sp from above is immediately used.
- If PulseRate1 (Speed input 1 from the pulse rate input) > TA_Spd_Sp the internal value Trp_Anticptr is set properly.
- If the I/O pack is configured for steam turbine application (internal value SteamTurbOnly), then TA_Trip (signal space) equals the value of Trp_Anticptr.

Note The I/O pack mounted on a TREA does not toggle the relays for trip anticipate function.



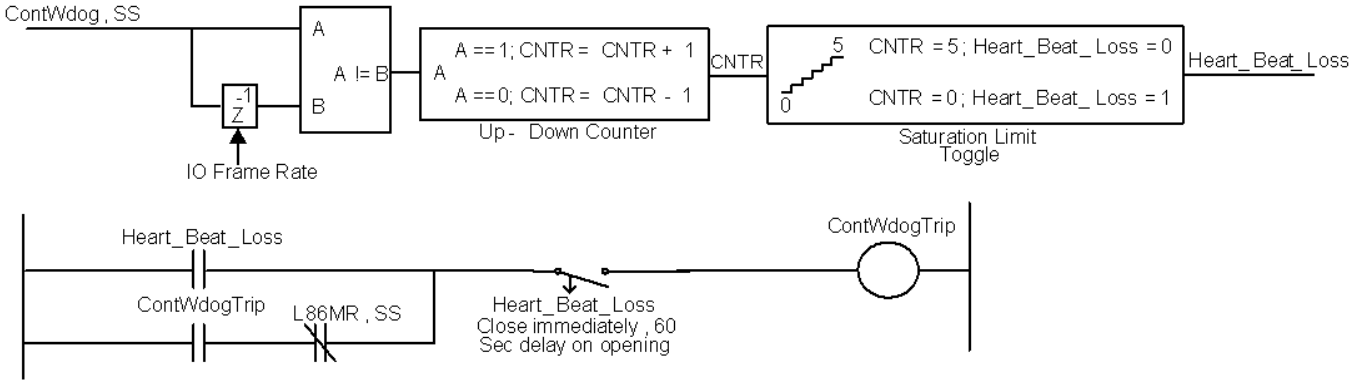
6.1.3.18 Solenoid Voltage / Power Sense

The I/O pack provides three comparator voltage inputs used to monitor solenoid power or solenoid voltage depending on the trip card that is connected. SOL1_Vfdbk (SS), SOL2_Vfdbk (SS), and SOL3_Vfdbk (SS) are generated from the input signals.

6.1.3.19 Main Control Watchdog

A standard control watchdog function is provided by the I/O pack. In this function, a value from a Device Heartbeat (DEVICE_HB) block is passed from the main controller to the I/O pack each data frame. If the I/O pack stops detecting the value from the main controller, a counter is incremented and, after five data frames, leads to a trip. If the main controller recovers for 60 seconds, the trip is removed, allowing for the recovery of the main controller with subsequent re-arming of the backup protection. The recovery function is provided for typical activities such as cycling power on a controller to perform maintenance.

While the controller is offline, the I/O pack associated with that controller will vote to trip. When the controller returns to operation, the I/O pack will remove the vote to trip. The watchdog offers monitoring of two main controllers in the event both Ethernet ports are connected. When configured for two controllers, having one controller active is sufficient to prevent a trip.



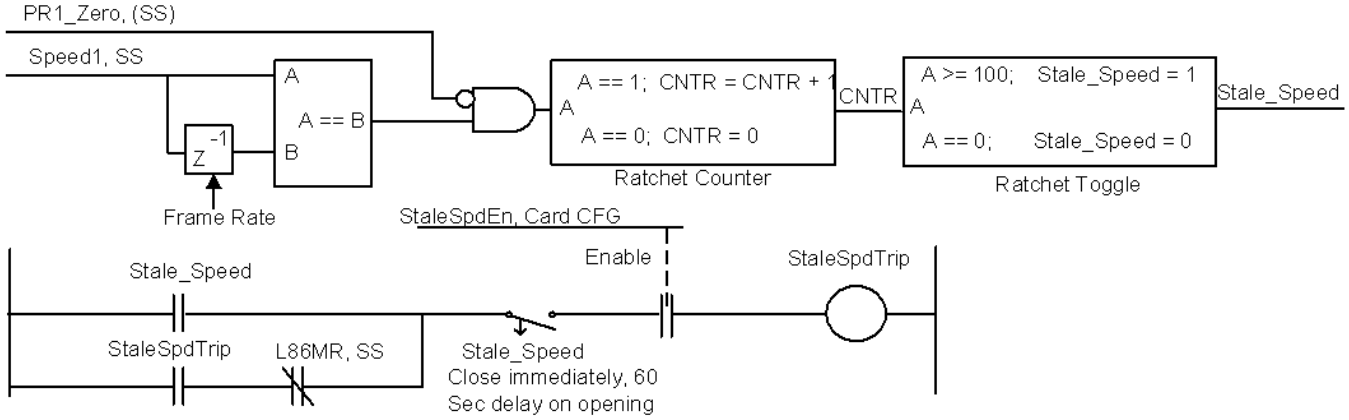
6.1.3.20 Stale Speed Detection

The I/O pack provides an additional main control watchdog function that is based on a live speed signal. The protection works as follows: If the pack PulseRate1 is determined to be zero speed the protection is turned off. If above zero speed, the pack looks at the value of Speed1 from the main control. If the most recent Speed1 value exactly matches the Speed1 value from the last data frame then a counter is incremented. If the counter reaches a threshold then a stale speed trip is declared and latched. If speeds are different the counter is cleared.

Attention

Although Speed_1, SS is available as a connected variable, it should not be forced. It can cause the protection to trip the system if enabled.

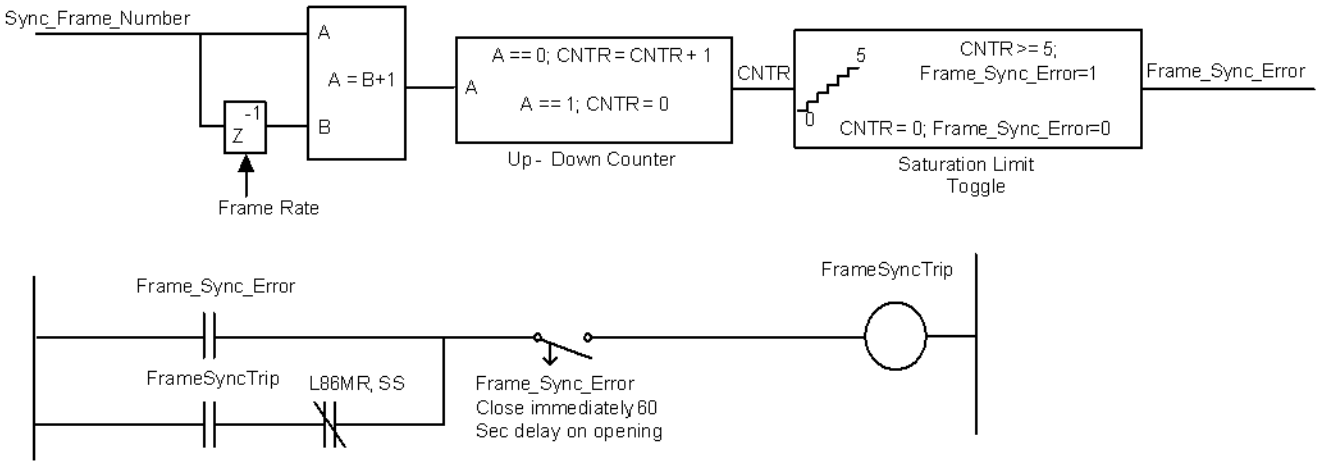
This protection is based on the knowledge that a live speed signal always *dithers* or moves some small amount. If the speed values being read by PPRO from the controller are not changing (dithering), there is loss of speed signal integrity from the controller. If the main control recovers for 60 seconds, the trip is removed allowing for the recovery of the main control with subsequent re-arming of the backup protection. The protection offers monitoring of two main controls in the event both Ethernet ports are connected. When configured for two controls, having one control satisfy the test is sufficient to prevent a trip.



6.1.3.21 Main Control Ethernet Monitor

The main control provides time synchronization across the distributed control elements. The time synchronization is tied tightly into the time at which traffic occurs on a given controller's IONet. The I/O pack provides monitoring of this service to ensure it is working correctly. Gross errors in time synchronization are detected by the pack through a number of different means, and if problems persist, the I/O pack will vote to trip. Once the trip is latched, if the problem goes away for 60 seconds the trip shall be reset (this assumes the control recovers from the problem and is back on line). The monitor will offer monitoring of two main controls in the event both Ethernet ports are connected. When configured for two controls, having one control sequencing correctly is sufficient to prevent a trip.

In the following diagram, the detection has been simplified to display monitoring of an Ethernet frame number as the means for determining a problem is present.

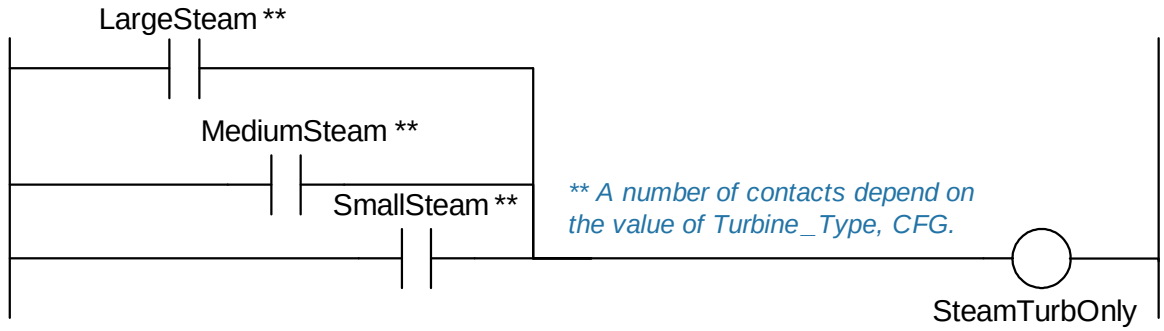


Sync Frame Count Monitor

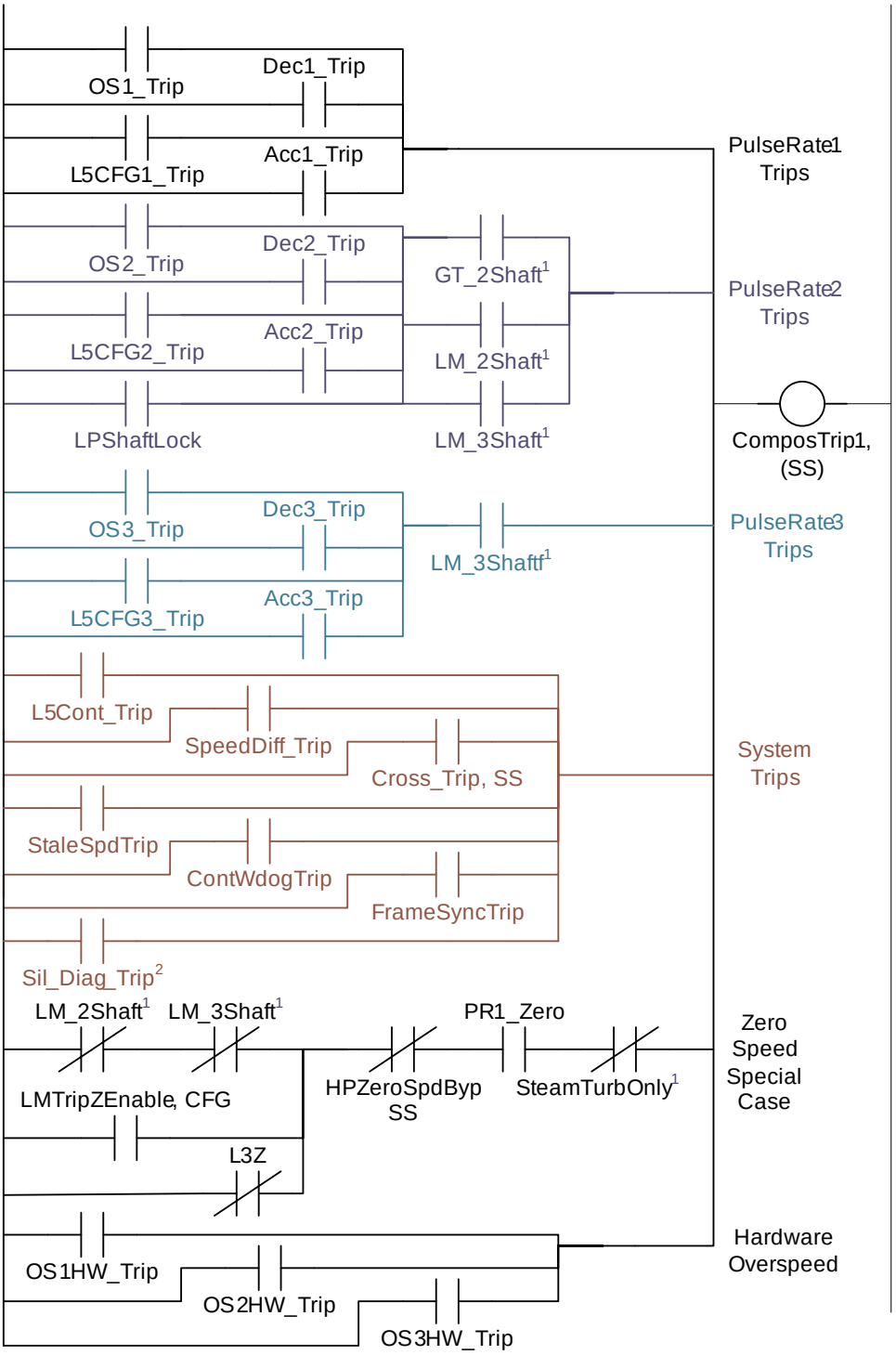
6.1.3.22 Trip Signal Logic

The different trip signals are combined into a composite signal that is used in the relay output logic. The following figure specifies how the signals are combined. This function is partitioned between firmware and programmable logic. The path to trip through hardware overspeed is done completely in hardware so that a firmware malfunction cannot defeat the protection. The same is true of the contact input trip signals when they are configured for direct trip.

There are differences between steam turbine protection and other protection. A composite signal SteamTurbOnly is created for ease of use:



Steam Turbine Trip Signals



Notes: [1] CFG values.

[2] This trip is generated if a *PulseRate* signal is broken (such as in the case of no signal) and *SilMode* is set to enabled, or if a hardware issue is detected regardless of *SilMode*. There will be an accompanying diagnostic generated to designate the actual cause of the trip

Trip Combine - All Signals (SS) unless Marked

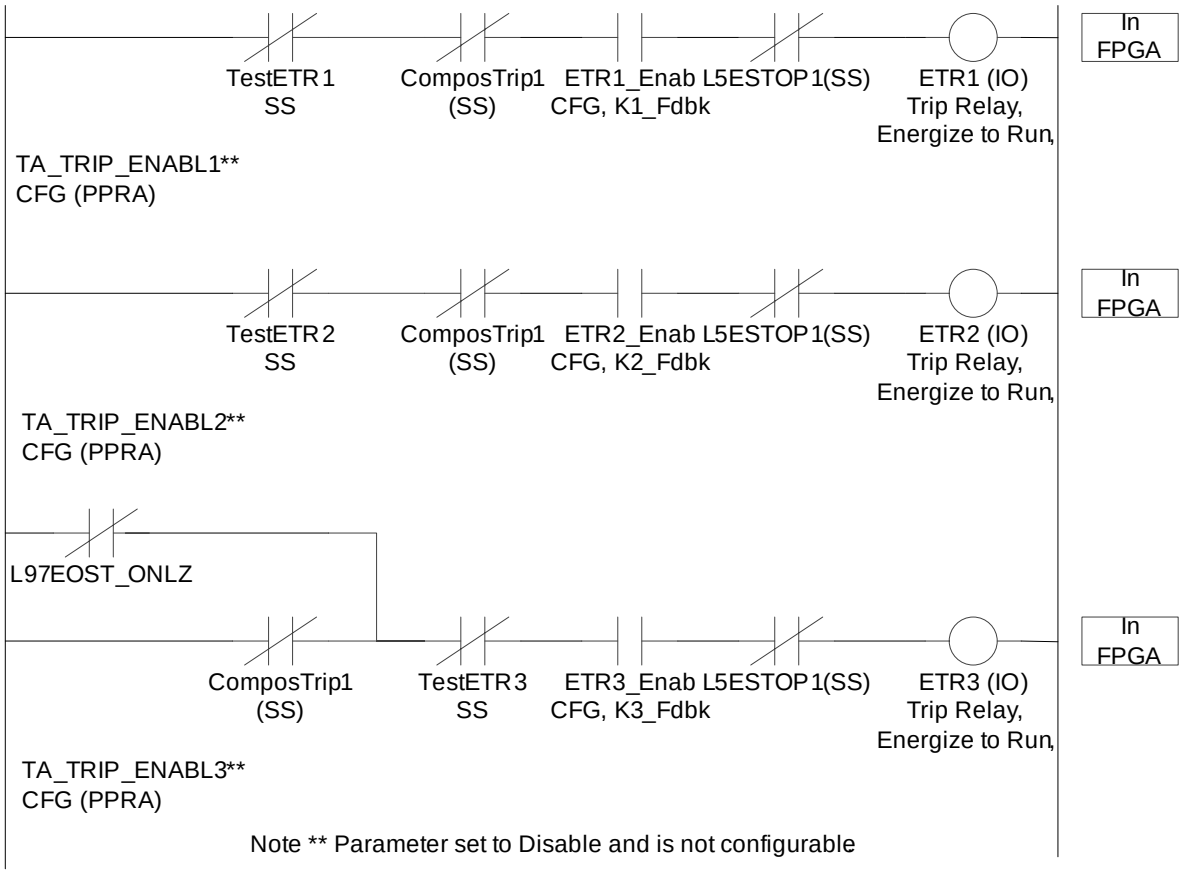
6.1.3.23 Watchdog Trip Function

Hardware in the I/O pack monitors local firmware operation, providing a watchdog trip function if the firmware malfunctions. The operation of this watchdog does not display in the normal sequencing figures. The I/O pack hardware is designed to be in a fail-safe or trip mode if it is not properly configured and operating. This means that with power off, while starting up, when in a hardware reset, or otherwise not online, the I/O pack will vote to trip. If the I/O pack watchdog acts, it resets the hardware thereby generating a vote to trip.

The processor board used inside the I/O pack has hardware features that allow it to differentiate between a reset caused by the watchdog hardware and a reset caused by cycling of power. This information is available from the pack after it restarts. In the event that an I/O pack votes to trip due to a reset, it is then possible to determine if a watchdog reset or a cycling of control power caused the event.

6.1.3.24 Trip Relay Outputs

PPRA provides drivers for three emergency trip relay commands, and provides monitoring for three status feedback signals. Trip is a combination of firmware trip and direct trip implemented in programmable logic.



Trip and Economizing Relay Outputs

6.1.4 Specifications

Item	PPRA Specification
Speed input quantity	Six input signals provided
Speed input range	Pulse rate frequency range 2 Hz to 20 kHz
Speed input accuracy	Pulse rate accuracy 0.05% of reading
Speed input sensitivity Speed input sensitivity is such that turning gear speed may be observed on a typical turbine application.	Required peak-peak (p-p) voltage rises as a function of frequency: 2 Hz requires 28 mV p-p 20 kHz requires 300 mV p-p
Frame Rate	100 Hz maximum
Size	8.26 cm High x 4.19 cm Wide x 12.1 cm Deep (3.25 in x 1.65 in x 4.78 in)
Technology	Surface-mount
† Ambient rating for enclosure design	PPRAS1B is rated from -40 to 70ºC (-40 to 158 ºF) PPRAS1A and PPRAH1A are rated from -30 to 65ºC (-22 to 149 ºF)

Note † For further details, refer to the *Mark VIe and Mark VIeS Control Systems System Guide, Volume I* (GEH-6721_Vol_I), the chapter *Technical Regulations, Standards, and Environments*.

6.1.5 Diagnostics

The I/O pack performs the following self-diagnostic tests:

- A power-up self-test that includes checks of RAM, flash memory, Ethernet ports, and most of the processor board hardware
- Continuous monitoring of the internal power supplies for correct operation
- A check of the analog feedback currents
- A comparison between the commanded state of each relay drive and the feedback from the commanded output circuit
- A check of the electronic ID information from the terminal board, acquisition board, and processor board to confirm that the hardware set matches, followed by a check that the application code loaded from flash memory is correct for the hardware set.

A failed power-up self-test is indicated by solid red lighting of the power and attention LEDs. Failure to verify the electronic ID will result in a communication failure. Failures of the other tests will result in a generated diagnostic alarm.

Details of the individual diagnostics are available from the ToolboxST application. The diagnostic signals can be individually latched, and then reset with the RSTDIAG if they become inactive.

6.1.5.1 PPRA Trip Status

Six additional LEDs located on the left side of the faceplate are used for trip status. All six LEDs stay off until all hardware application is complete. The LEDs indicate trip status of the PPRA as follows:

RUN is green any time the I/O pack has energized the emergency trip relays. RUN turns red any time the I/O pack has removed power from the emergency trip relays, voting to trip.

ESTP is green when the E-STOP input (if applicable) is in the run state. ESTP turns red any time E-STOP is invoked to prevent pick up of the emergency trip relays. If the chosen trip terminal board doesn't support E-STOP then the LED defaults to green.

OSPD turns red any time the I/O pack votes to trip in response to a detected overspeed condition on any of the three speed inputs. OSPD is green when an overspeed condition is not present or latched.

WDOG turns red when any of the following PPRA trip functions are enabled and active:

- Control Watch dog
- Speed Difference Detection
- Stale Speed Detection
- Frame Sync Monitor

WDOG turns green to indicate that the trip status of any of these features has been cleared.

SIL is green when configured for SIL 2 or SIL 3 safety functionality. When configured for SIL 3 if an internal fault is detected, it turns red. PPRAS1A and S1B with TREAS1A and WREAS1A are required for SIL functionality.

Note The SIL and KREA LEDs are only labeled on the PPRAS1A, but are also present on the H1A version.

KREA is green when power is detected on the KREA sub-module in the I/O pack.

During normal PPRA operation, all six application LEDs display green. An additional feature, rotating LEDs, can be configured for the PPRA. Using this feature, only one LED is turned on at a time and walked up and down the six LEDs creating a synchronized motion. The walking is regulated by the controller IONet and synchronized across a set of three I/O packs. This provides a quick visual indication of the system time synchronization status.

6.1.6 Configuration

The following subsections (Parameters, Pulse Rate, Contacts, E-Stop, ETR Relays, Variables, and so forth) define the choices within the tabs of the ToolboxST configuration.

6.1.6.1 Parameters

Parameter	Description	Choices
TurbineType	Turbine Type and Trip Solenoid Configuration	Unused, GT_1Shaft, LM_ 3Shaft, MediumSteam, SmallSteam,GT_2Shaft, Stag_ GT_1Sh,Stag_GT_2Sh, LM_ 2Shaft
LMTripZEnabl	On LM machine, when no PR on Z,Enable a vote for Trip	Disable, Enable
SpeedDifEn	Enable Trip on Speed Difference between Controller and PPRA	Disable, Enable
StaleSpdEn	Enable Trip on Speed from Controller Freezing	Disable, Enable
RotateLeds	Rotate the Status LEDs if all status are OK	Disable, Enable
LedDiags	**Attention** **LedDiags is Disabled by default.** When enabled, generates a diagnostic alarm when Trip LEDs are lit. Refer to the section, Diagnostics, *PPRA Trip Status* for more information on LED operation.	Disable, Enable
SilMode	Perform additional SIL diagnostic and trip checks	Not_SIL, SIL_2,SIL_3
PRGrouping	Whether the six speed inputs are grouped as 3 groups of two (three shafts) or 2 groups of three (two shafts)	ThreeGroups, TwoGroups
RatedRPM_TA	Rated RPM, used for Trip Anticipater and for Speed Diff Protection	0 to 20,000
AccelCalTime	Select Acceleration Calculation Time (milliseconds)	10 to 100
OS_Diff	Absolute Speed Difference in Percent For Trip Threshold	0 to 10
HwSpdDiff Sensitivity	How quickly a trip is caused when the speed differs within a group	Normal, High, Low

6.1.6.2 Pulse Rate

Parameter	Description	Choices
PRType	Selects the type of Pulse Rate Input, (For Proper Resolution)	Unused, Speed, Flow, Speed_LM, Speed_High
PRScale	Pulses per Revolution (outputs RPM)	0 to 1,000
OSHW_Setpoint	Hardware Overspeed Trip Setpoint in RPM	0 to 20,000
OS_Setpoint	Overspeed Trip Setpoint in RPM	0 to 20,000
OS_Tst_Delta	Off Line Overspeed Test Setpoint Delta in RPM	-2,000 to 2,000
Zero_Speed	Zero Speed for this Shaft in RPM (1 RPM hysteresis), 0 RPM sets PR#_Zero always false	0 to 20,000
Min_Speed	Min Speed for this Shaft in RPM	0 to 20,000
Accel_Trip	Enable Acceleration Trip	Disable, Enable
Acc_Setpoint	Acceleration Trip Setpoint in RPM / Sec	0 to 20,000
TMR_DiffLimt	Diag Limit,TMR Input Vote Difference, in Eng Units	0 to 20,000
Dual_DiffLimit	Diag Limit,Dual speed sensor, in Eng Units	0 to 20,000

6.1.6.3 Contacts

Parameter	Description	Choices
ContactInput	ContactInput	Used, Unused
SeqOfEvents	Record Contact transitions in Sequence of Events	Enable, Disable
DiagVoteEnab	Enable Voting Disagreement Diagnostic	Enable, Disable
TripMode	TripMode	Enable, Disable

6.1.6.4 E-Stop (Used on TREA)

Parameter	Description	Choices
EstopEnab	Enable E-Stop Detection on TREA	Enable, Disable
DiagVoteEnab	Enable Voting Disagreement Diagnostic	Enable, Disable

6.1.6.5 ETR Relays

Parameter	Description	Choices
RelayOutput	Relay Signal	Used, Unused
DiagVoteEnab	Enable Voting Disagreement Diagnostic	Enable, Disable
DiagSolEnab	Enable Solenoid Voltage Diagnostic	Enable, Disable

6.1.6.6 Variables PPRA

Variable	Description	Direction	Type
L3DIAG_PPRA_R,_S, and _T	I/O Diagnostic Indication	Input	BOOL
LINK_OK_PPRA_R,_S, and _T	I/O Link Okay Indication	Input	BOOL
ATTN_PPRA_R,_S, and _T	I/O Attention Indication	Input	BOOL
PS18V_PPRA_R,_S, and _T	I/O 18 V Power Supply Indication	Input	BOOL
PS28V_PPRA_R,_S, and _T	I/O 28 V Power Supply Indication	Input	BOOL
IOPackTmpr_R,_S, and _T	I/O Pack Temperature (deg °F)	AnalogInput	REAL
K1FLT	K1 Shorted Contact Fault	Input	BOOL
K2FLT	K2 Shorted Contact Fault	Input	BOOL
K3FLT	K3 Shorted Contact Fault	Input	BOOL
Repeater_flt1	RS-232 Speed repeater fault for PR4_Spd	Input	BOOL
Repeater_flt2	RS-232 Speed repeater fault for PR5_Spd	Input	BOOL
Repeater_flt3	RS-232 Speed repeater fault for PR6_Spd	Input	BOOL
SilModErr	Sil Mode Configuration modification after going On Line	Input	BOOL
EstopModErr	E-Stop Configuration modification after going On Line	Input	BOOL
TA_StptLoss	L30TA	Input	BOOL
GT_1Shaft	Config – Gas Turb,1 Shaft Enabled	Input	BOOL
GT_2Shaft	Config – Gas Turb,2 Shaft Enabled	Input	BOOL
LM_2Shaft	Config – LM Turb,2 Shaft Enabled	Input	BOOL
LM_3Shaft	Config – LM Turb,3 Shaft Enabled	Input	BOOL
MediumSteam	Config – Medium Steam Enabled	Input	BOOL
SmallSteam	Config – Small Steam Enabled	Input	BOOL
Stag_GT_1Sh	Config – Stag 1 Shaft, Enabled	Input	BOOL
Stag_GT_2Sh	Config – Stag 2 Shaft, Enabled	Input	BOOL
L3SS_Comm	Communication Status - OK = True	Input	BOOL
LokdRotorByp	LL97LR_BYP - Locked Rotor Bypass	Output	BOOL
HPZeroSpdByp	L97ZSC_BYP - HP Zero Speed Check Bypass	Output	BOOL
Speed1	Shaft Speed 1 in RPM	AnalogOutput	REAL
ContWdog	Controller Watchdog Counter	Output	DINT

6.1.6.7 Variables Contacts

Variable	Contact Variable Description	Direction	Type
Contact1	Contact Input 1	Input	BOOL
Contact2	Contact Input 2	Input	BOOL
Contact3	Contact Input 3	Input	BOOL
Contact4	Contact Input 4	Input	BOOL

6.1.6.8 Variables E-Stop

Variable	Description	Direction	Type
KESTOP1_Fdbk	ESTOP1,inverse sense,True = Run	Input	BOOL

6.1.6.9 Variables ETR Relays

Variable	Description	Direction	Type
K1_Fdbk	L4ETR1_FB, Trip Relay 1 Feedback	Input	BOOL
K2_Fdbk	L4ETR2_FB, Trip Relay 2 Feedback	Input	BOOL
K3_Fdbk	L4ETR3_FB, Trip Relay 3 Feedback	Input	BOOL

6.1.6.10 Variables Fanned-PR

Variable	Description	Direction	Type
Fan_Spd_Fbk	Fanned Speed Signal Feedback: Fanned = Jumpers Closed	Input	BOOL

6.1.6.11 Variables Pulse Rate

Variable	Description	Direction	Type
PulseRate1	HP speed	AnalogInput	REAL
PulseRate2	LP speed	AnalogInput	REAL
PulseRate3	IP speed	AnalogInput	REAL

6.1.6.12 Variables Vars-CI

Variable	Description	Direction	Type
Cont1_TrEnab	Config – Contact 1 Trip Enabled – Direct	Input	BOOL
Cont2_TrEnab	Config – Contact 2 Trip Enabled – Direct	Input	BOOL
Cont3_TrEnab	Config – Contact 3 Trip Enabled – Direct	Input	BOOL
Cont4_TrEnab	Config – Contact 4 Trip Enabled – Direct	Input	BOOL
Inhbt1_Fdbk	Trip Inhibit Signal Feedback for Contact 1	Input	BOOL
Inhbt2_Fdbk	Trip Inhibit Signal Feedback for Contact 2	Input	BOOL
Inhbt3_Fdbk	Trip Inhibit Signal Feedback for Contact 3	Input	BOOL
Inhbt4_Fdbk	Trip Inhibit Signal Feedback for Contact 4	Input	BOOL
Trip1_EnCon	Contact 1 Trip Enabled – Conditional	Input	BOOL
Trip2_EnCon	Contact 2 Trip Enabled – Conditional	Input	BOOL
Trip3_EnCon	Contact 3 Trip Enabled – Conditional	Input	BOOL
Trip4_EnCon	Contact 4 Trip Enabled – Conditional	Input	BOOL
Trip1_Inhbt	Contact 1 Trip Inhibit	Output	BOOL
Trip2_Inhbt	Contact 2 Trip Inhibit	Output	BOOL
Trip3_Inhbt	Contact 3 Trip Inhibit	Output	BOOL
Trip4_Inhbt	Contact 4 Trip Inhibit	Output	BOOL

6.1.6.13 Variables Vars-Relay

Variable	Description	Direction	Type
K1_FdbkNV_R, S, T	Non Voted L4ETR1_FB, Trip Relay 1 Feedback	Input	BOOL
K2_FdbkNV_R, S, T	Non Voted L4ETR2_FB, Trip Relay 2 Feedback	Input	BOOL
K3_FdbkNV_R, S, T	Non Voted L4ETR3_FB, Trip Relay 3 Feedback	Input	BOOL
ETR1_Enab	Config – ETR1 Relay Enabled	Input	BOOL
ETR2_Enab	Config – ETR2 Relay Enabled	Input	BOOL
ETR3_Enab	Config – ETR3 Relay Enabled	Input	BOOL
PTR1	L20PTR1 - Primary Trip Relay CMD versus Voltage - a Mismatch Diagnostic Monitor	Output	BOOL
PTR2	L20PTR2 - Primary Trip Relay CMD versus Voltage - a Mismatch Diagnostic Monitor	Output	BOOL
PTR3	L20PTR3 - Primary Trip Relay CMD versus Voltage - a Mismatch Diagnostic Monitor	Output	BOOL
TestETR1	L97ETR1 - ETR1 test, True de-energizes relay	Output	BOOL
TestETR2	L97ETR2 - ETR2 test, True de-energizes relay	Output	BOOL
TestETR3	L97ETR3 - ETR3 test, True de-energizes relay	Output	BOOL

6.1.6.14 Variables Vars-Speed

Variable	Vars-Speed Variable Description	Direction	Type
Acc1_TrEnab	Config – Accel 1 Trip Enabled	Input	BOOL
Acc2_TrEnab	Config – Accel 2 Trip Enabled	Input	BOOL
Acc3_TrEnab	Config – Accel 3 Trip Enabled	Input	BOOL
OS1HW_SP_Pend	Hardware HP overspeed setpoint changed after power up	Input	BOOL
OS2HW_SP_Pend	Hardware LP overspeed setpoint changed after power up	Input	BOOL
OS3HW_SP_Pend	Hardware IP overspeed setpoint changed after power up	Input	BOOL
OS1HW_SP_CfgErr	Hardware HP Overspd Setpoint Config Mismatch Error	Input	BOOL
OS2HW_SP_CfgErr	Hardware LP Overspd Setpoint Config Mismatch Error	Input	BOOL
OS3HW_SP_CfgErr	Hardware IP Overspd Setpoint Config Mismatch Error	Input	BOOL
OS1_SP_CfgEr	HP Overspd Setpoint Config Mismatch Error	Input	BOOL
OS2_SP_CfgEr	LP Overspd Setpoint Config Mismatch Error	Input	BOOL
OS3_SP_CfgEr	IP Overspd Setpoint Config Mismatch Error	Input	BOOL
PR1_Accel	HP Accel in RPM/SEC	AnalogInput	REAL
PR2_Accel	LP Accel in RPM/SEC	AnalogInput	REAL
PR3_Accel	IP Accel in RPM/SEC	AnalogInput	REAL
PR1_Max	HP Max Speed since last Zero Speed in RPM	AnalogInput	REAL
PR2_Max	LP Max Speed since last Zero Speed in RPM	AnalogInput	REAL
PR3_Max	IP Max Speed since last Zero Speed in RPM	AnalogInput	REAL
PR1_Spd	PR1 - Speed sensor 1 (1A if three or two groups, see PRGrouping parameter)	AnalogInput	REAL
PR2_Spd	PR2 - Speed sensor 2 (2A if three groups, 1B if two groups, see PRGrouping parameter)	AnalogInput	REAL
PR3_Spd	PR3 - Speed sensor 3 (3A if three groups, 2A if two groups, see PRGrouping parameter)	AnalogInput	REAL
PR4_Spd	PR4 - Speed sensor 4 (1B if three groups, 1C if two groups, see PRGrouping parameter)	AnalogInput	REAL
PR5_Spd	PR5 - Speed sensor 5 (2B if three or two groups, see PRGrouping parameter)	AnalogInput	REAL
PR6_Spd	PR6 - Speed sensor 6 (3B if three groups, 2C if two groups, see PRGrouping parameter)	AnalogInput	REAL
OnLineOS1Tst	L97HP_TST1 - On Line HP Overspeed Test	Output	BOOL
OnLineOS2Tst	L97LP_TST1 - On Line LP Overspeed Test	Output	BOOL
OnLineOS3Tst	L97IP_TST1 - On Line IP Overspeed Test	Output	BOOL
OffLineOS1Tst	L97HP_TST2 - Off Line HP Overspeed Test	Output	BOOL
OffLineOS2Tst	L97LP_TST2 - Off Line LP Overspeed Test	Output	BOOL

Variable	Vars-Speed Variable Description	Direction	Type
OffLineOS3Tst	L97IP_TST2 - Off Line IP Overspeed Test	Output	BOOL
PR_Max_Rst	Max Speed Reset	Output	BOOL
OnLineOS1X	L43EOST_ONL - On Line HP Overspeed Test,with auto reset	Output	BOOL
OS1_Setpoint	HP Overspeed Setpoint in RPM	AnalogOutput	REAL
OS2_Setpoint	LP Overspeed Setpoint in RPM	AnalogOutput	REAL
OS3_Setpoint	IP Overspeed Setpoint in RPM	AnalogOutput	REAL
OS1_TATrpSp	PR1 Overspeed Trip Setpoint in RPM for Trip Anticipate Fn	AnalogOutput	REAL
OSHW_Setpoint1	HP Overspeed Setpoint in RPM	AnalogOutput	REAL
OSHW_Setpoint2	LP Overspeed Setpoint in RPM	AnalogOutput	REAL
OSHW_Setpoint3	IP Overspeed Setpoint in RPM	AnalogOutput	REAL

6.1.6.15 Variables Vars-Trip

Variable	Vars-Trip Variable Description	Direction	Type
ComposTrip1	Composite Trip 1	Input	BOOL
WatchDog_Trip	Enhanced diag - Watch Dog trip	Input	BOOL
StaleSpeed_Trip	Enhanced diag - Stale Speed trip	Input	BOOL
SpeedDiff_Trip	Enhanced diag - Speed Difference trip	Input	BOOL
FrameMon_Flt	Enhanced diag - Frame Monitor Fault	Input	BOOL
Sil_Diag_Trip	SIL Diagnostic Trip	Input	BOOL
PR1_Zero	L14HP_ZE - HP shaft at zero speed	Input	BOOL
PR2_Zero	L14LP_ZE - LP shaft at zero speed	Input	BOOL
PR3_Zero	L14IP_ZE - IP shaft at zero speed	Input	BOOL
OS1_Trip	L12HP_TP - HP overspeed trip	Input	BOOL
OS2_Trip	L12LP_TP - LP overspeed trip	Input	BOOL
OS3_Trip	L12IP_TP - IP overspeed trip	Input	BOOL
Dec1_Trip	L12HP_DEC - HP de-acceleration trip Can only be reset when pulses are able to be seen on speed input or after the I/O pack is rebooted.	Input	BOOL
Dec2_Trip	L12LP_DEC - LP de-acceleration trip Can only be reset when pulses are able to be seen on speed input or after the I/O pack is rebooted.	Input	BOOL
Dec3_Trip	L12IP_DEC - IP de-acceleration trip Can only be reset when pulses are able to be seen on speed input or after the I/O pack is rebooted.	Input	BOOL
Acc1_Trip	L12HP_ACC - HP acceleration trip	Input	BOOL

Variable	Vars-Trip Variable Description	Direction	Type
Acc2_Trip	L12LP_ACC - LP acceleration trip	Input	BOOL
Acc3_Trip	L12IP_ACC - IP acceleration trip	Input	BOOL
DualCfgErr	Dual sensor cfg mismatch - SIL 3 will trip in 1 hour	Input	BOOL
OS1HW_Trip	L12HP_HTP - HP Hardware detected overspeed trip	Input	BOOL
OS2HW_Trip	L12LP_HTP - LP Hardware detected overspeed trip	Input	BOOL
OS3HW_Trip	L12IP_HTP - IP Hardware detected overspeed trip	Input	BOOL
HW_Spd1_diff	HW speed diff PR1 detected - SIL 3 will trip in 1 hour	Input	BOOL
HW_Spd2_diff	HW speed diff PR2 detected - SIL 3 will trip in 1 hour	Input	BOOL
HW_Spd3_diff	HW speed diff PR3 detected - SIL 3 will trip in 1 hour	Input	BOOL
L5CFG1_Trip	HP Config Trip	Input	BOOL
L5CFG2_Trip	LP Config Trip	Input	BOOL
L5CFG3_Trip	IP Config Trip	Input	BOOL
L5CFG3_Trip	E-STOP1 Trip	Input	BOOL
L5Cont1_Trip	Contact 1 Trip	Input	BOOL
L5Cont2_Trip	Contact 2 Trip	Input	BOOL
L5Cont3_Trip	Contact 3 Trip	Input	BOOL
L5Cont4_Trip	Contact 4 Trip	Input	BOOL
LPShaftLock	LP Shaft Locked	Input	BOOL
Cross_Trip	L4Z_XTRP - Control Cross Trip	Output	BOOL

6.1.6.16 Variables VSen

Variable	Description	Direction	Type
VSen1	Voltage Sensor 1 Feedback	Input	BOOL
VSen2	Voltage Sensor 2 Feedback	Input	BOOL
VSen3	Voltage Sensor 3 - Power Monitor Feedback	Input	BOOL

6.2 PPRA Specific Alarms

The following alarms are specific to the PPRA I/O pack.

40

Description Contact Excitation Voltage Test Failure

Possible Cause Voltage for the contact inputs on the trip board is not within published limits.

Solution Check source of contact excitation voltage applied to trip board.

50

Description Main Terminal Board Mismatch

Possible Cause

- The terminal board that was selected in the ToolboxST configuration does not match the actual board found by the PPRA.
- The WREA daughterboard has not been attached to the TREA.

Solution

- Change the ToolboxST configuration to use the correct board.
- Replace the terminal board to match the board selected in the ToolboxST configuration.
- Verify that the WREA is seated correctly on the TREA.

51

Description TREA board mismatch - remain offline

Possible Cause The TREA hardware grouping is not compatible with the Sil Capable IS200PPRAS1A I/O pack. The PPRA will not go online in this state.

Solution

- Verify that you are using a IS220PPRAS1A module attached to a TREA SxA/WREA SxA terminal board.
- Either use a SIL capable terminal board or replace the PPRA with an IS200PPRAH1A.

52

Description Grouped speed inputs require fanned speed input jumpers to be in place

Possible Cause The JP1 and JP2 jumpers are not set to fan the speed signals to all three packs. This is required for grouped speed inputs.

Solution Remove the WREA daughterboard, and set the jumpers to the correct position.

53

Description WREA - Repeater status fault 1/4

Possible Cause The speed repeater output does not match the input speed signal.

- One of the speed sensors is not connected.
- The pins on the cable are shorted.
- The RS-232/RS-485 chip is not functioning.

Solution

- Verify the pins and connections on the cable.
- Verify the connection of both speed sensors.
- Replace the WREA daughterboard.

54

Description WREA - Repeater status fault 2/5

Possible Cause The speed repeater output does not match the input speed signal.

- One of the speed sensors is not connected.
- The pins on the cable are shorted.
- The RS-232/RS-485 chip is not functioning.

Solution

- Verify the pins and connections on the cable.
- Verify the connection of both speed sensors.
- Replace the WREA daughterboard.

55

Description WREA - Repeater status fault 3/6

Possible Cause The speed repeater output does not match the input speed signal.

- One of the speed sensors is not connected.
- The pins on the cable are shorted.
- The RS-232/RS-485 chip is not functioning.

Solution

- Verify the pins and connections on the cable.
- Verify the connection of both speed sensors.
- Replace the WREA daughterboard.

56

Description Dual speed sensors mismatch: PR 1=[ ], PR 4=[ ]

Possible Cause The dual speed sensors are reporting speeds that differ by more than the configured **Dual_DiffLimit** value.

Solution

- Verify that the **Dual_DiffLimit** value is set correctly. Note that the value is given in engineering units.
- Verify the connection and correct operation of the speed sensors.

57

Description Dual speed sensors mismatch: PR 2=[ ], PR 5=[ ]

Possible Cause The dual speed sensors are reporting speeds that differ by more than the configured **Dual_DiffLimit** value.

Solution

- Verify that the **Dual_DiffLimit** value is set correctly. Note that the value is given in engineering units.
- Verify the connection and correct operation of the speed sensors.

58

Description Dual speed sensors mismatch: PR 3=[ ], PR 6=[ ]

Possible Cause The dual speed sensors are reporting speeds that differ by more than the configured **Dual_DiffLimit** value.

Solution

- Verify that the **Dual_DiffLimit** value is set correctly. Note that the value is given in engineering units.
- Verify the connection and correct operation of the speed sensors.

59

Description Internal power supply failure - P5 power for WREA

Possible Cause The PPRA internal 5 V power supply is unhealthy, causing either a faulty PPRA or TREA+WREA terminal board.

Solution

- If all three PPRAs are reporting the problem, replace the TREA+WREA terminal board.
- If only one pack is reporting the problem, replace the PPRA.

60

Description Internal power supply failure - P15 power for WREA

Possible Cause The PPRA internal 15 V power supply is unhealthy, causing either a faulty PPRA or TREA+WREA terminal board.

Solution

- If all three PPRAs are reporting the problem, replace the TREA+WREA terminal board.
- If only one pack is reporting the problem, replace the PPRA.

61

Description Internal power supply failure - N15 power for WREA

Possible Cause The PPRA internal -15 V power supply is unhealthy causing either a faulty PPRA or TREA+WREA terminal board.

Solution

- If all three PPRAs are reporting the problem, replace the TREA+WREA terminal board.
- If only one pack is reporting the problem, replace the PPRA.

62-64

Description Hardware speed mismatch: PR[ ], PR[ ]

Possible Cause The FPGA detected differences between speed sensors. SIL3 systems will be tripped in one hour.

Solution

- SIL 3 systems will trip the emergency trip relays one hour after this condition has been detected.
- Check the connection and correct the operation of the speed sensors.

65

Description Configuration changed after power up - running with old configuration

Possible Cause The following configuration parameters may not change after going online:

- **EstopEnab**
- **SILMode**
- **PRType** cannot go from/to Unused
- **PRScale**
- Contact Input TripMode/Used/Unused
- **PRGrouping**
- **SpdDiffSensitivity**

Note This restriction is in place even if *SilMode* is set to *Not_Sil* due to hardware restrictions in the PPRA.

Solution

- Check if the listed parameters have been changed inadvertently. Refer to the error log. From the ToolboxST application, right-click **IOPack** and select **Troubleshooting**, **Advanced Diagnostics**, and **Error Log**.
- Set the parameters to their original state and download them to the PPRA if they have been changed inadvertently.
- Remove power from the I/O pack to get the hardware to accept the new values if changes are required.

66

Description PPRA is not SIL compatible - remain offline

Possible Cause One or more of the PPRA(s) are not SIL compatible. The PPRA module will not go online in this condition.

Solution

- Verify that the BPPB or BPPC, BPRO, KREA, TREA, and WREA are all *S* board revision types. Replace all *H* board revisions with their *S* board revisions.
- Change the *SilMode* parameter to *Not_SIL*.

69-71

Description Trip Relay (ETR) Driver [ ] does not match commanded state

Possible Cause The driver output of the I/O pack for Emergency Trip Relay 1 (K1), ETR2 (K2), or ETR3 (K3) does not match the commanded state. This indicates that the I/O pack does not see the relay command going out the DC-62 connector into the expected terminating impedance on the trip board.

Solution

- Check the I/O pack connector seating on the terminal board.
- Check the trip board cable seating (if not TREA) and the cable integrity.
- Replace the cable, the trip board, the main terminal board, and the I/O pack.

72-74

Description Econ Relay Driver [ ] does not match commanded state

Possible Cause The driver output of the I/O pack for Economizing Relay KE1, KE2, or KE3 does not match the commanded state. This indicates that the I/O pack does not see the relay command going out the DC-62 connector into the expected terminating impedance on the trip board.

Solution

- Check the I/O pack connector seating on terminal board.
- Check the trip board cable seating and the cable integrity.
- Replace the cable, the trip board, the main terminal board, and the I/O pack.

75

Description Servo Clamp Relay Driver does not match commanded state

Possible Cause The driver output of I/O pack for K4CL does not match the commanded state. This indicates that I/O pack does not see the relay command going out the DC-62 connector into the expected terminating impedance on the trip board.

Solution

- Check the I/O pack connector seating on terminal board.
- Check the trip board cable seating and the cable integrity.
- Replace the cable, the trip board, the main terminal board, and the I/O pack.

76

Description K25A Relay (synch check) Driver does not match commanded state

Possible Cause The driver output of I/O pack for K25A does not match the commanded state. This indicates that I/O pack does not see the relay command going out the DC-62 connector into the expected terminating impedance on the trip board.

Solution

- Check the I/O pack connector seating on terminal board.
- Check the trip board cable seating and the cable integrity.
- One at a time, replace the following: the emergency trip board cable, the trip terminal board, the terminal board hosting the I/O pack, and the I/O pack.

83-85

Description Trip Relay (ETR) Contact [ ] does not match commanded state

Possible Cause

- Relay feedback from Emergency Trip Relay ETR1 (K1), ETR2 (K2), or ETR3 (K3) does not match the commanded state. This indicates that the relay feedback from the trip board does not agree with the commanded state.
- Solenoid power is not applied to the trip board.

Solution

- Check the trip board relays, as well as the cable from trip board to main terminal board (if not TREA).
- Check that solenoid power is applied to the terminal board.

86-88

Description Econ Relay Contact [ ] does not match commanded state

Possible Cause The relay feedback from Economizing Relay 1 (KE1), KE2, or KE3 does not match the commanded state. This indicates that the relay feedback from the trip board does not agree with the commanded state.

Solution Check the trip board relays, as well as the cable from trip board to main terminal board.

89

Description Servo Clamp Relay Contact does not match commanded state

Possible Cause The relay feedback from K4CL does not match the commanded state. This indicates that the relay feedback from the trip board does not agree with the commanded state.

Solution

- Check the I/O pack connector seating on the terminal board.
- Check the trip board cable seating and the cable integrity.
- Replace the cable, the trip board, the main terminal board, and the I/O pack.

90

Description K25A Relay Coil Feedback does not match commanded state

Possible Cause The relay feedback from K25A does not match the commanded state. This indicates that the relay feedback from the trip board does not agree with the commanded state. Relay feedback is taken after hardware command voting on the trip terminal board has occurred; therefore, a probable cause is that one I/O pack is not commanding the same state as the other two I/O packs.

Solution

- Confirm that the TMR packs are commanding the same state for K25A.
- Check the I/O pack connector seating on the terminal board.
- Check the trip board cable seating and the cable integrity.
- One at a time, replace the following: the emergency trip board cable, the trip terminal board, the terminal board hosting the I/O pack, and the I/O pack.

97

Description Solenoid Power Source is missing

Possible Cause Solenoid power monitoring provided by the trip board indicates the absence of power.

Solution

- Check the source of solenoid power.
- Confirm that the wiring between the trip boards is correct.

99-101

Description Solenoid Voltage [ ] does not match commanded state

Possible Cause

- The solenoid voltage associated with K1-K3 does not match the commanded state.
- K1-K3 are closed, but no voltage is detected on the solenoid.
- Solenoid voltage was removed through another means while the I/O pack expects to detect its presence.
- The ETR state associated with this PPRA is being out voted by the other two PPRAs.

Solution

- Review the system-level trip circuit wiring and confirm the voltage should be present if the I/O pack energizes the associated trip relay.
- From the ToolboxST application, verify that the variables (typically L20PTR#) which drive the Primary Trip Relays (PTRs) in the PTUR are correctly assigned to the PPRO or PPRA Variables tab (PTR1, PTR2, and PTR3).
- Check the pre-voted values for *ComposTrip1* under the **Vars-Trip** tab to verify that all three PPRAs have the same status. If the current PPRA differs from the others, check the pre-vote status of other variables under this tab to determine the exact cause of the composite trip, and correct the condition.

105

Description TREL/S, Solenoid Power, Bus A, Absent

Possible Cause TRES/TREL solenoid power A is absent. Solenoid power does not match the solenoid state for longer than 40 milliseconds.

Solution

- Check power applied to the trip board.
- Check the field wiring.
- Check the solenoid.
- Replace the terminal board.

106

Description TREL/S, Solenoid Power, Bus B, Absent

Possible Cause TRES/TREL solenoid power B is absent. The solenoid power does not match the solenoid state for longer than 40 milliseconds.

Solution

- Check power applied to the trip board.
- Check the field wiring.
- Check the solenoid.
- Replace the terminal board.

107

Description TREL/S, Solenoid Power, Bus C, Absent

Possible Cause TRES/TREL solenoid power C is absent. The solenoid power does not match The solenoid state for longer than 40 milliseconds.

Solution

- Check power applied to the trip board.
- Check the field wiring.
- Check the solenoid.
- Replace the terminal board.

6.2.1 108

Description Control Watchdog Protection Activated

Possible Cause An alarm indicates that the *ContWdog* variable has not changed for five consecutive frames. The alarm clears if changes are seen for 60 seconds.

Solution

- Verify that the *ContWdog* is connected to the output of a *device_hb* block and that the block is located in a task which is run at frame rate.
- Verify that the output signal from the block is changing at least once a frame.

6.2.2 109

Description Speed Difference Protection Activated

Possible Cause This alarm only occurs if the parameter **SpeedDifEnable** has been enabled. An alarm indicates that the difference between the output signal *Speed1* and the first I/O pack pulse rate speed is larger than the percentage *OS_DIFF* for more than three consecutive frames. The percentage is based off of the parameter **RatedRPM_TA**. The alarm clears if the difference is within limits for 60 seconds for more than three consecutive frames.

Solution Verify that the *Speed1* signal is set up correctly in the ToolboxST and that the source of the signal reflects the primary (PTUR/YTUR) pulse rate speed.

6.2.3 110

Description Stale Speed Protection Activated

Possible Cause The speed trip protection may be stale. This alarm can only occur if the parameter **StaleSpdEn** has been enabled. An alarm indicates that the variable *Speed1* has not changed for 100 consecutive frames. The alarm clears if the speed dithers for 60 seconds.

Solution Verify that the *Speed1* signal is set up correctly in the ToolboxST configuration, and that the source of the signal reflects the primary (PTUR/YTUR) pulse rate speed.

6.2.4 111

Description Frame Sync Monitor Protection Activated

Possible Cause This alarm indicates that the communication with the controller was lost for at least five consecutive frames after the I/O pack was online. The alarm clears if the frame synch is established for at least 60 seconds.

Solution Verify that the IONet is healthy. This indicates that the I/O pack is not synchronized with the Mark VIe start-of-frame signal.

112-114

Description Overspeed [ ] firmware setpoint configuration error

Possible Cause There is a firmware overspeed limit mismatch between IO signal space limit and the configuration. The current configuration file downloaded from the ToolboxST application has a different over-speed limit than the IO signal **OS[ ]_Setpoint**.

Solution Change the output signal designated in **OS[ ] _Setpoint** (**Vars-Speed** tab) to match the configuration value **OS_ Setpoint** (**Pulse Rate** tab).

115-117

Description Overspeed [ ] hardware setpoint configuration error

Possible Cause There is a hardware over-speed limit mismatch between IO signal space limit and the configuration. The current configuration file downloaded from the ToolboxST application has a different over-speed limit than the IO signal **OSHW_Setpoint[ ]**.

Solution Change the output signal designated in **OSHW_ Setpoint [ ]** (**Vars-Speed** tab) to match the configuration value in **OSHW_Setpoint** (**Pulse Rate** tab).

118-120

Description Overspeed [ ] hardware setpoint changed after power up

Possible Cause

- This alarm always occurs when Pulse Rate [ ] **HWOS_Setpoint** is changed and downloaded to the I/O pack after the turbine has started.
- It can also change if **PRScale** is changed to a decimal value and downloaded to the I/O pack after the turbine has started.

Solution

- Confirm that the limit or scale change is correct.
- Restart the I/O pack to force the hardware overspeed to re-initialize the limit.

121

Description TREA - K1 solid state relay shorted

Possible Cause The TREA provides voltage-based detection of relays that remain in the energized position in the six voting contacts used to provide K1. Zero voltage has been detected on one or more contacts of K1 when voltage should be present.

Solution Replace the TREA.

122

Description TREA - K2 solid state relay shorted

Possible Cause TREA provides voltage based detection of relays that remain in the energized position in the six voting contacts used to provide K2. Zero voltage has been deleted on one or more contacts of K2 when voltage should be present.

Solution Replace the TREA.

123

Description LED - Turbine RUN Permissives Lost

Possible Cause The RUN LED is lit red on the I/O pack because one of the RUN permissives for the turbine has been lost. The **LedDiags** parameter must be set to *Enable* to get this alarm.

Solution

- Verify the configuration of the **LedDiag** parameter.
- From the **Vars-Trip** tab, identify the condition that caused the trip.
- The condition leading to a trip condition must be cleared, and a master reset issued.

124

Description LED - Overspeed fault detected

Possible Cause The Overspeed LED is lit on the pack because of a detected Trip condition. The **LedDiag** parameter must be set to True to get this alarm.

Solution

- Verify the configuration of the **LedDiag** parameter.
- The condition leading to a trip condition must be cleared, and a master reset issued.

125

Description LED - Estop detected

Possible Cause The E-Stop LED is lit on the pack because of a detected E-Stop signal. The **LedDiag** parameter must be set to True to get this alarm.

Solution

- Verify the configuration of the **LedDiag** parameter.
- Remove the E-Stop condition and issue a master reset.

126

Description LED - SIL3 trip pending

Possible Cause The SIL trip pending LED is lit on the I/O pack because a hardware speed difference has been detected between two redundant sensors. The emergency trip relays (ETR) will fire one hour after the condition has been detected.

Solution

- SIL 3 systems will fire the ETR one hour after this condition has been detected. After resolving the issue, cycle power to the I/O pack to reset this alarm.
- Power down the I/O pack and determine the source of the sensor discrepancy.

127

Description WREA - K3 solid state relay shorted

Possible Cause WREA provides voltage based detection of "stuck-on" relays in the six voting contacts used to provide K3. Zero voltage has been deleted on one or more contacts of K3 when voltage should be present.

Solution Replace the WREA.

128

Description Tripped - Missing pulse rate signal

Note This diagnostic is generated from hardware detection that is only available on BPPC-based I/O packs. BPPB-based I/O packs will not detect this condition the same way.

Possible Cause No speed input detected on a speed sensor due to the following reasons:

- Broken wire
- Sensor malfunction
- Signal conditioning malfunction

Solution

- Check the terminal connections for the speed sensor.
- Check the speed sensor gap.

129

Description Processor hardware error detected (Error Code:[ ])

Possible Cause Hardware error detected by the FPGA due to the following reasons:

- Error code 1: FPGA program changed during runtime, possibly one-time event
- Error code 2: clock oscillator error

Note These conditions cause a trip that can only be cleared with a power cycle.

Solution

- Restart the I/O pack.
- Download the firmware of the I/O pack.
- If the problem persists, replace the I/O pack.

130

Description Invalid configuration detected

Possible Cause The configuration is not supported due to the following reasons:

- TREA not selected
- TRES/L is selected
- QC Mode enabled
- Configured as a Large Steam turbine

Note These conditions cause a trip that can only be cleared by changing the configuration and restarting the I/O pack.

Solution Change the configuration to be valid.

131-136

Description Speed sensor mismatch for PulseRate [ ]: PR[ ]_Spd [ ]

Possible Cause A speed sensor is reporting speeds that differ by more than the configured **Dual_DiffLimit** value from the voted PulseRate value.

Solution

- Verify that the **Dual_DiffLimit** value is set correctly (value is given in engineering units).
- Check the connection and correct the operation of the speed sensors.

137-143

Description Hardware speed sensor mismatch PR[ ], PR[ ]

Possible Cause The FPGA detected an excessive difference between speed sensors, and the **SilMode** parameter is set to SIL2 or SIL3. If SilMode is set to SIL3, then the system will trip in 1 hour.

Solution

- SIL 3 systems will trip the emergency trip relays one hour after this condition has been detected.
- Verify the connection and correct the operation of the speed sensors.
- If speed sensors appear to match but diagnostic is still active, reduce speed to less than 50% of the **HW_OS_Setpoint** to reset the diagnostic and trip condition.

144

Description PRGrouping of two groups is not supported by this module

Possible Cause The configuration has **PRGrouping** set to *TwoGroups* and is trying to run on an H1A/S1A. This configuration is not supported.

Solution Change **PRGrouping** to *ThreeGroups* or change the H1A/S1A module to an H1B/S1B module.

145

Description HwSpdDiffSensitivity setting invalid for this module

Possible Cause **HwSpdDiffSensitivity** is either Low or High. Only Normal is supported for H1A/S1A modules.

Solution Either change **HwSpdDiffSensitivity** to Normal or change the H1A/S1A module to an H1B/S1B module.

224-239

Description Input Signal [ ] Voting Mismatch, Local=[ ], Voted=[ ]

Possible Cause A problem exists with a status input between the R, S, and T I/O packs and one of the following:

- Device
- Connections to the terminal board
- Terminal board

Solution

- Adjust the TMR threshold limit or correct the cause of the difference.
- Verify that the R, S, and T I/O pack configurations are equal to the ToolboxST configuration.
- Check the I/O pack power and the networking.
- Check the I/O pack mounting on terminal board.
- Verify the operation of the device generating the specified signal.
- Verify the terminal board wiring and connections.
- Replace the I/O pack.

1064-1255

Description Logic Signal [ ] Voting Mismatch

Possible Cause A problem exists with a status input between the R, S, and T I/O packs and one of the following:

- Device
- Connections to the terminal board
- Terminal board

Solution

- Verify that the R, S, and T I/O pack configurations are equal to the ToolboxST configuration.
- Check the I/O pack power and the networking.
- Check the I/O pack mounting on the terminal board.
- Verify the operation of the device generating the specified signal.
- Verify the terminal board wiring and connections.
- Replace the I/O pack.